Cairn seminar — November 29th, 2013

Algorithms and arithmetic for the implementation of cryptographic pairings

Nicolas Estibals
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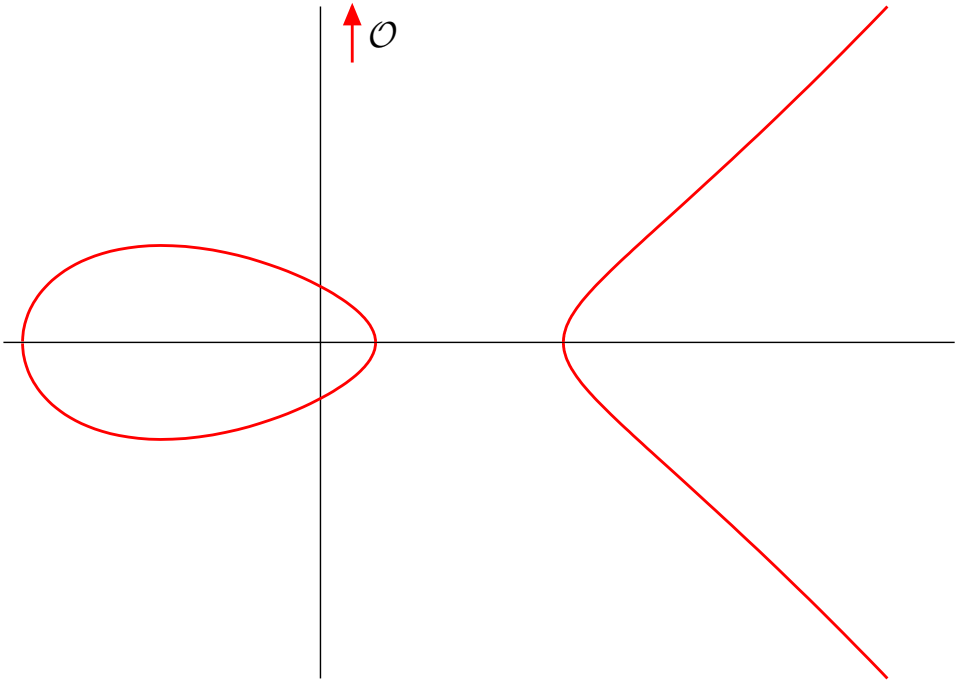
What is an elliptic curve?



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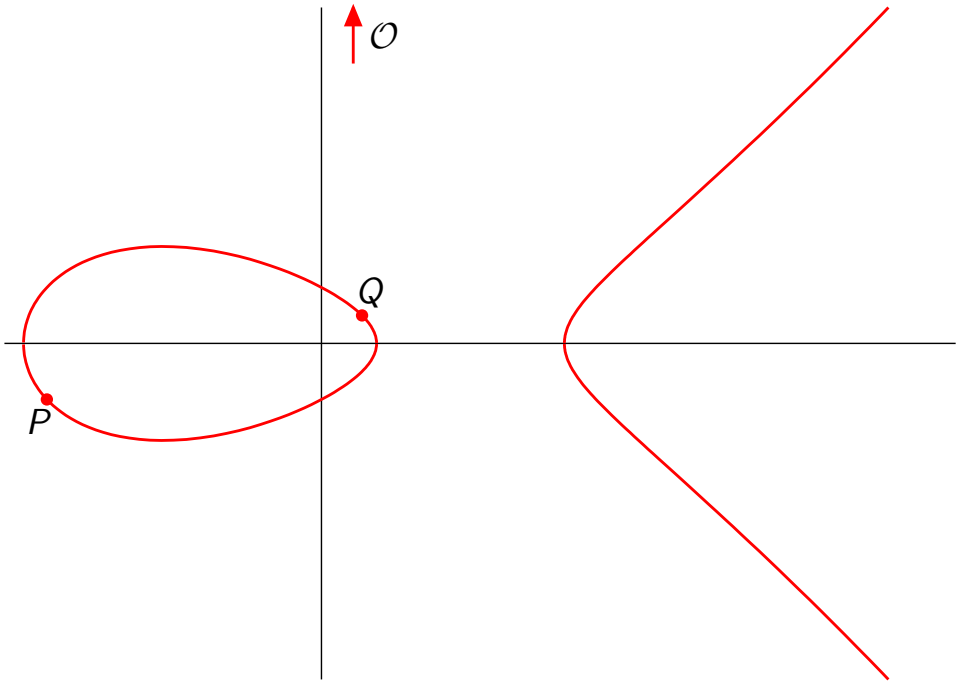

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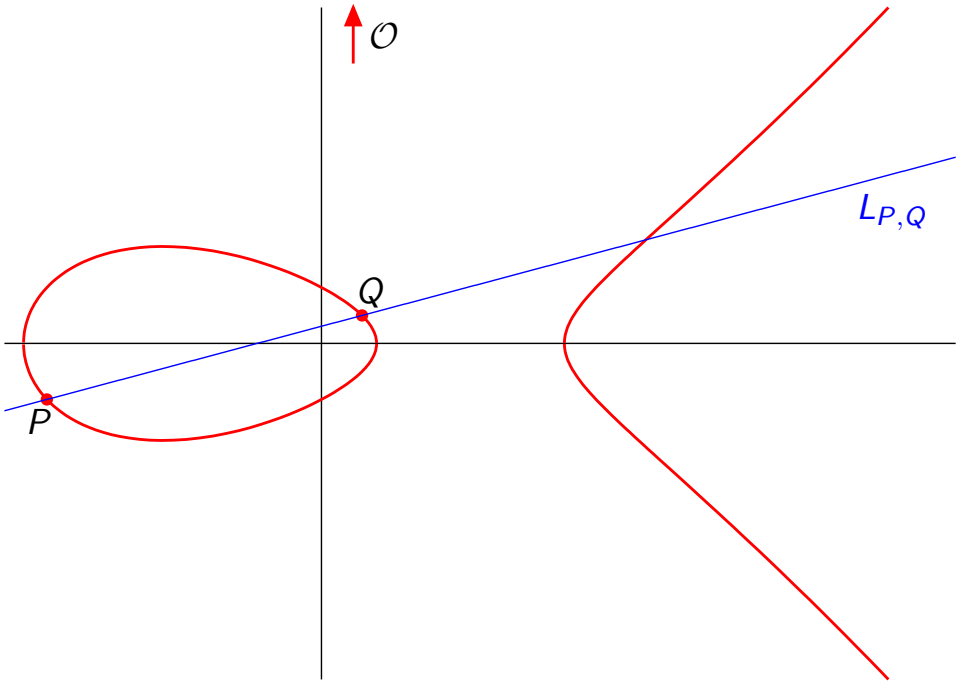

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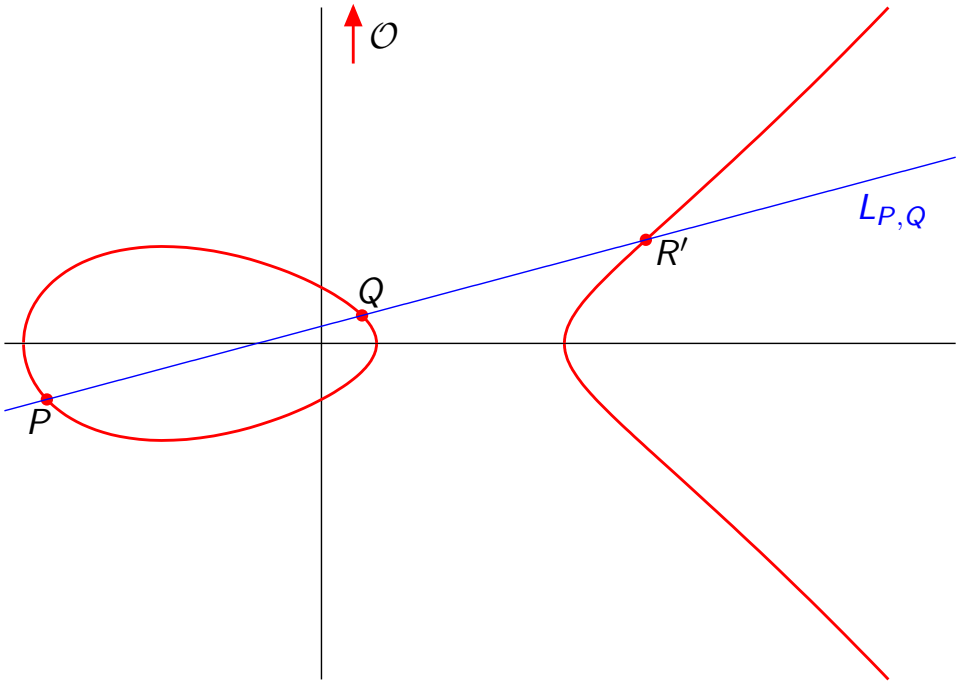

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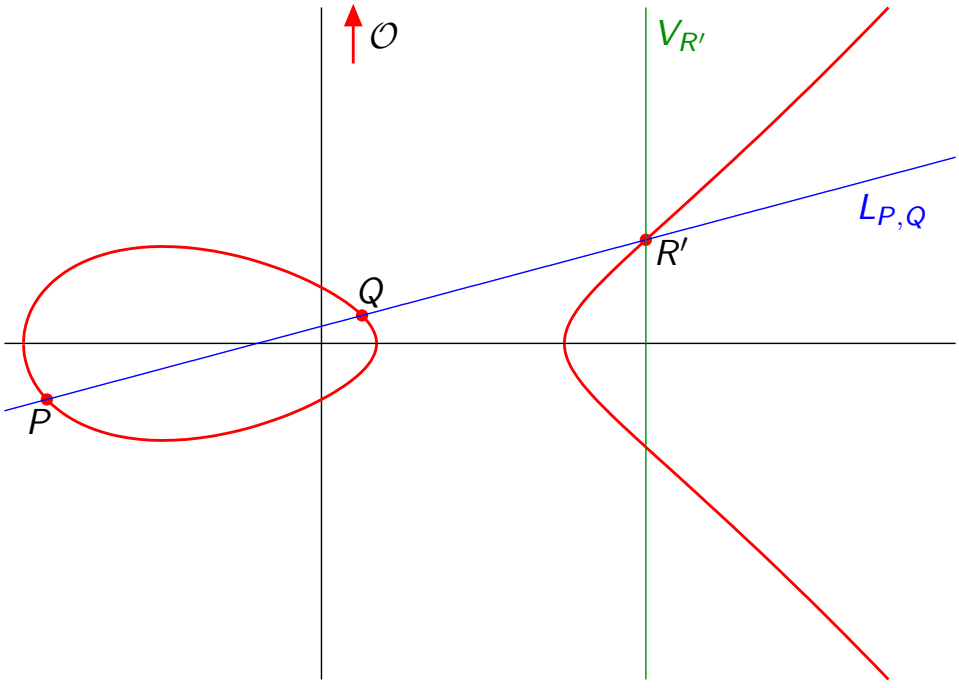

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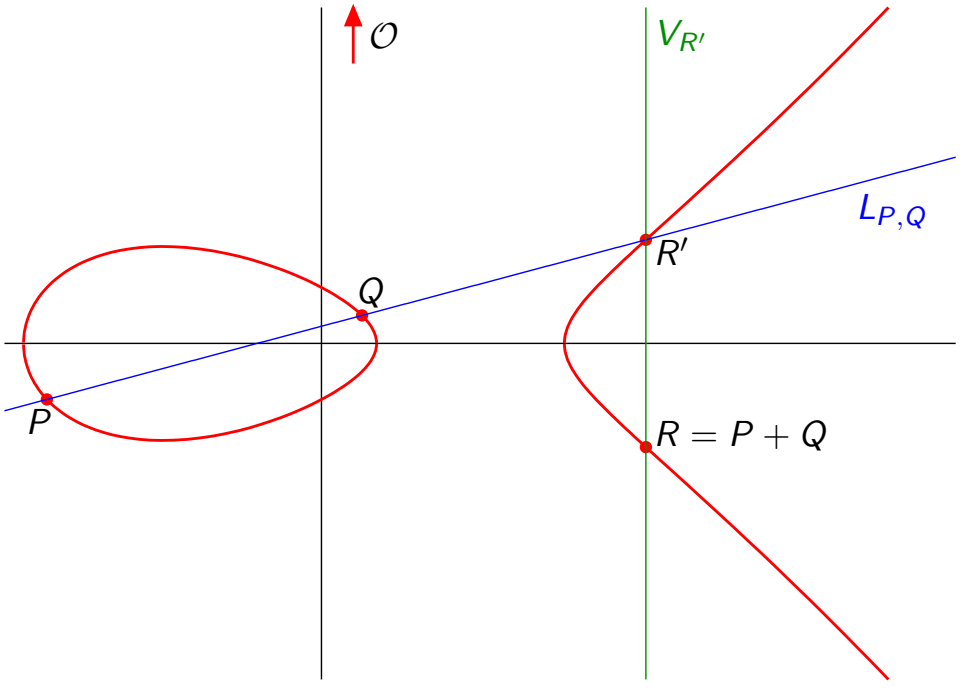

Elliptic Curve Cryptography

Discrete Logarithm Problem (DLP)

Let $\mathbb{G}$ be a cyclic group, P a generator, given $Q \in \mathbb{G}$, it is supposed to be hard to compute a such that

$$Q = [a]P$$

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Discrete Logarithm Problem (DLP)

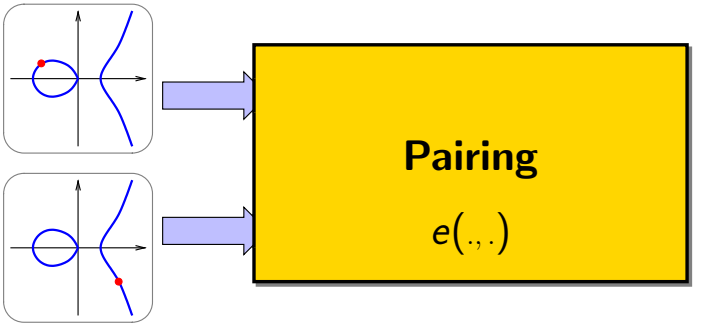
Let $\mathbb{G}$ be a cyclic group, P a generator, given $Q \in \mathbb{G}$, it is supposed to be hard to compute a such that

$$Q = [a]P$$

- Use this hard problem to design cryptographic protocols
- Diffie–Hellman key exchange:
  - Alice generates a secret integer a
  - Alice sends $[a]P$ to Bob
  - Alice computes $[a][b]P$
  - Bob generates a secret integer b
  - Bob sends $[b]P$ to Alice
  - Bob computes $[b][a]P$

They both share the same secret: $[ab]P$

What is a pairing?



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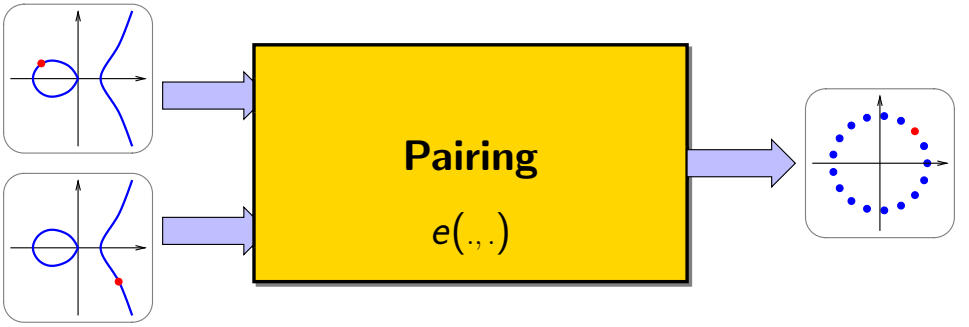

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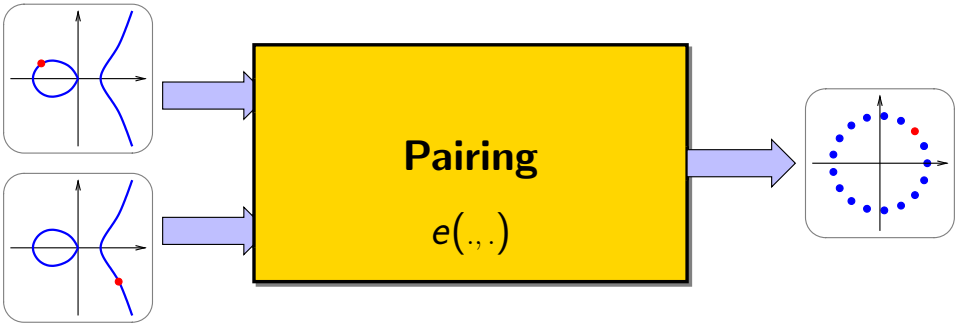

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$$e([a]P, [b]Q) = e(P, Q)^{ab}$$

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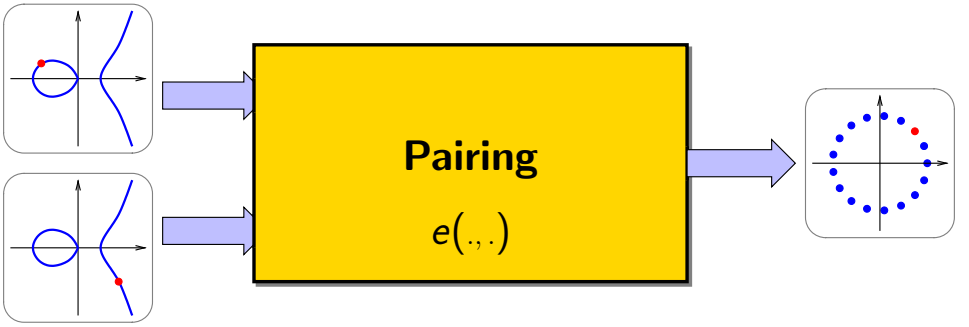

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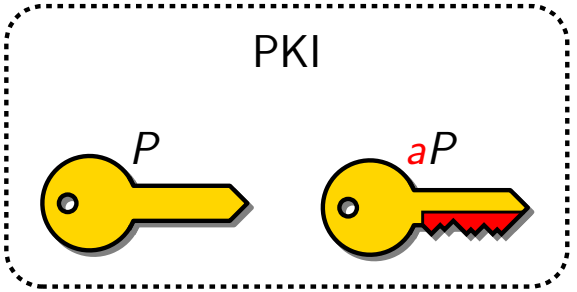
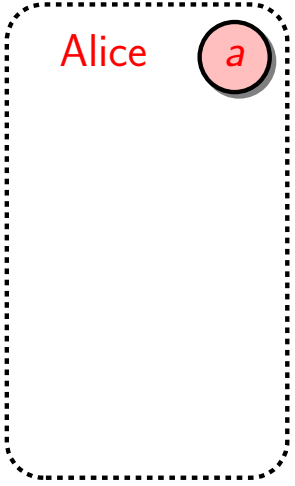
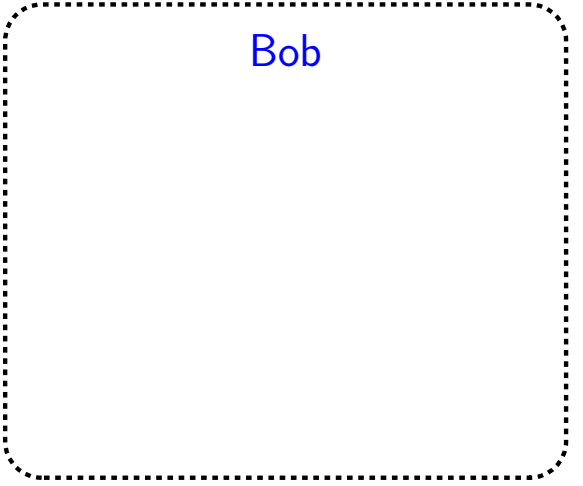
$$e([a]P, [b]Q) = e(P, Q)^{ab}$$

- Useful for advanced protocols
  - short signature
  - electronic voting
  - electronic money
  - ...

Example: Short signature







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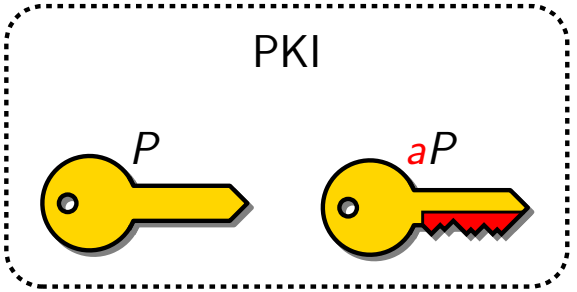

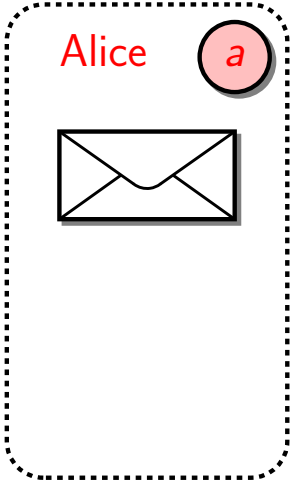

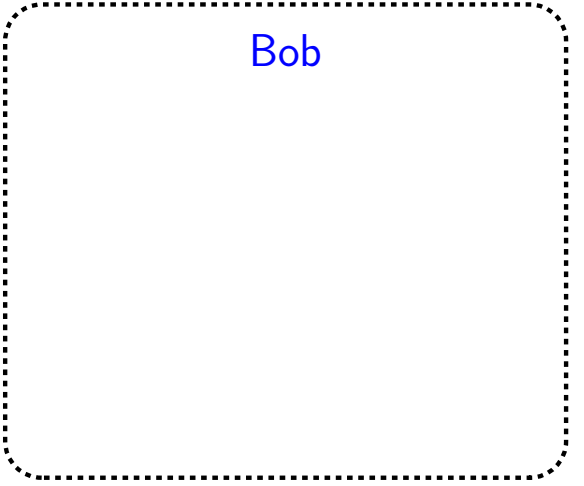

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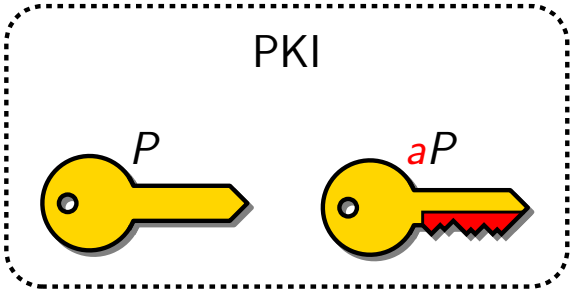

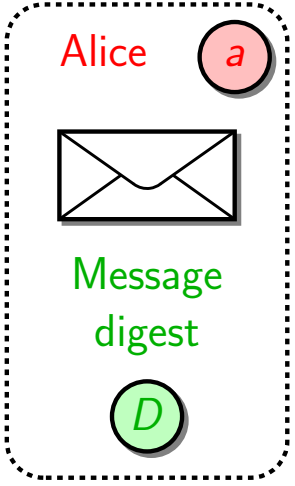

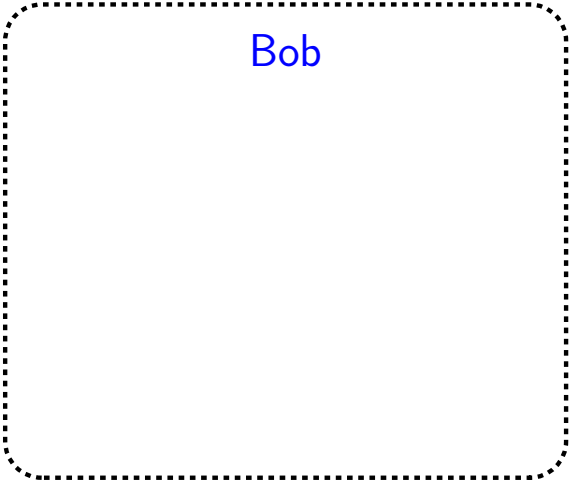

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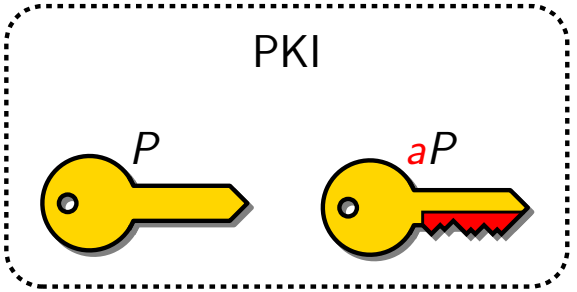

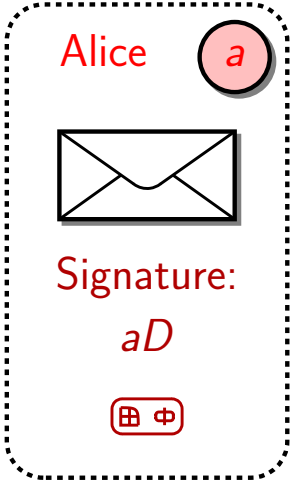

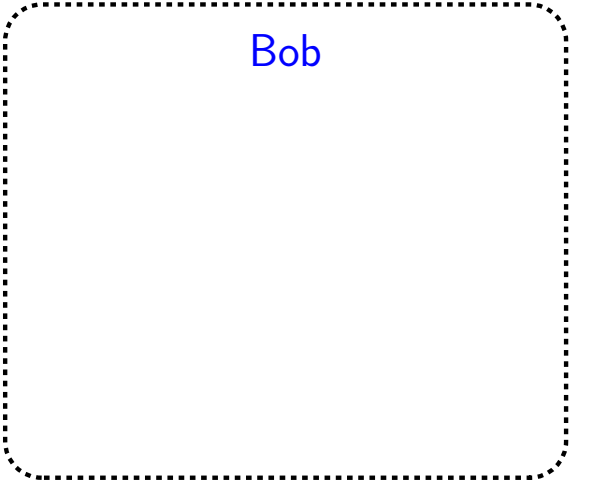

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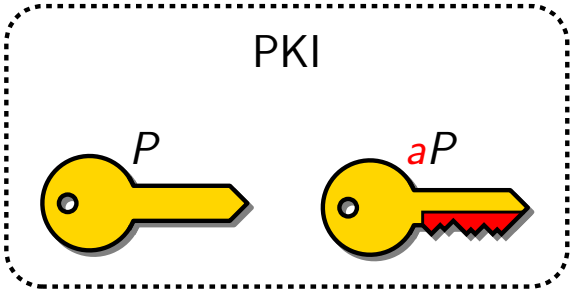

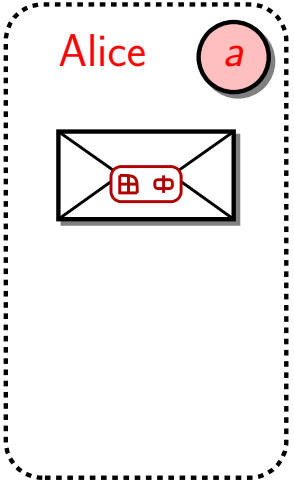

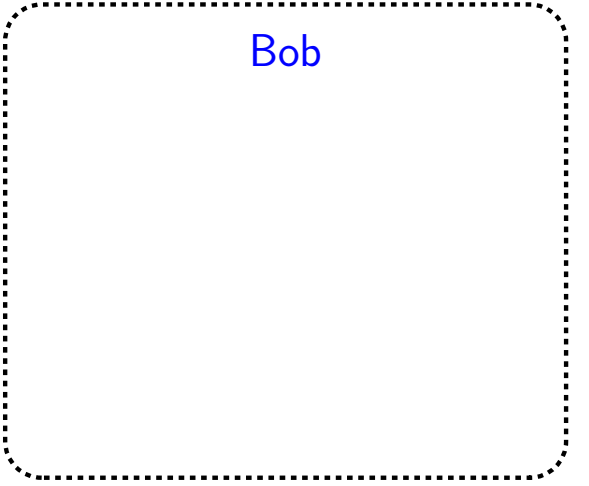

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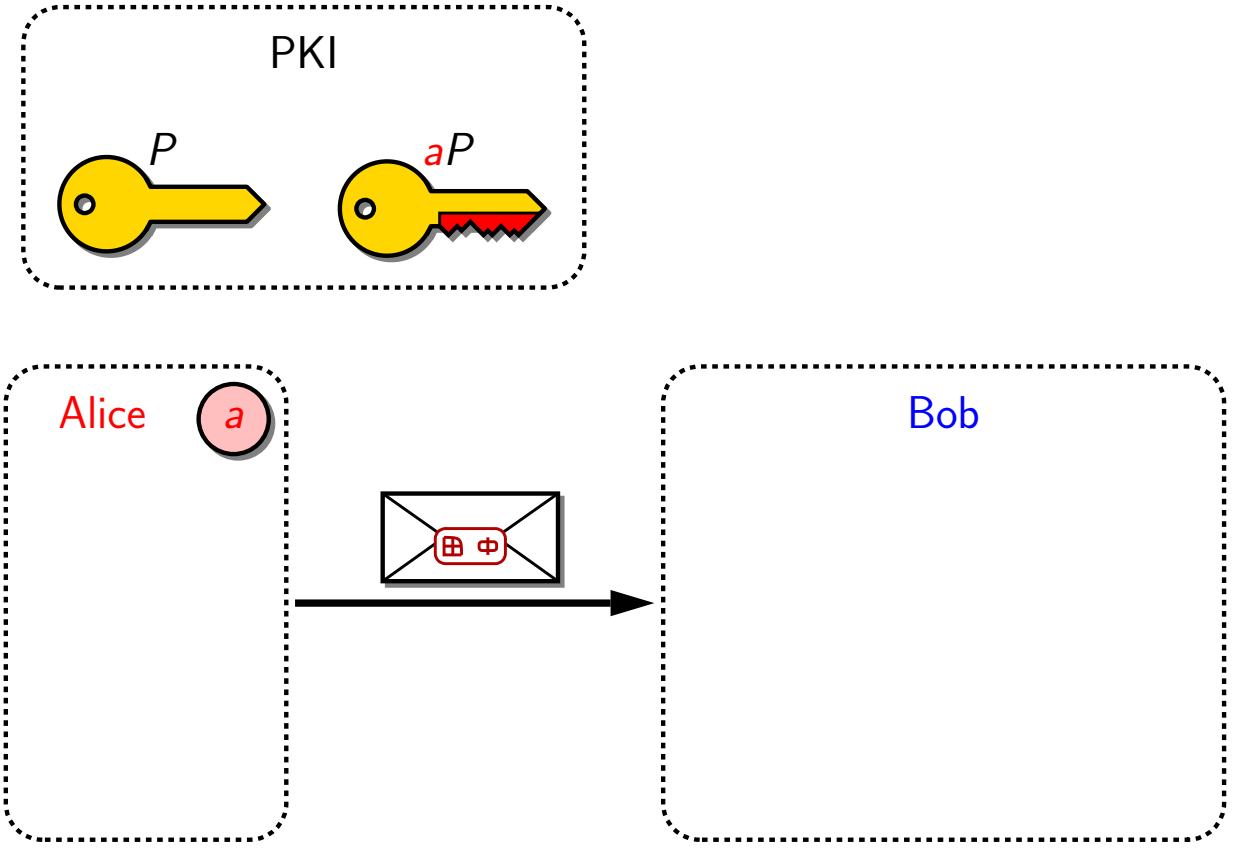

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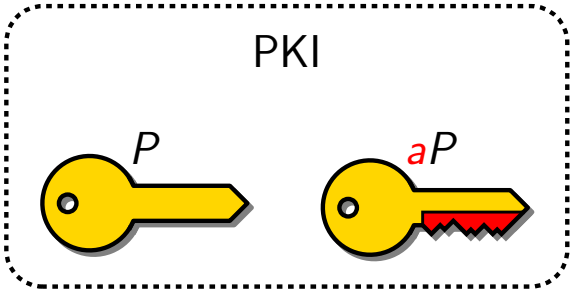

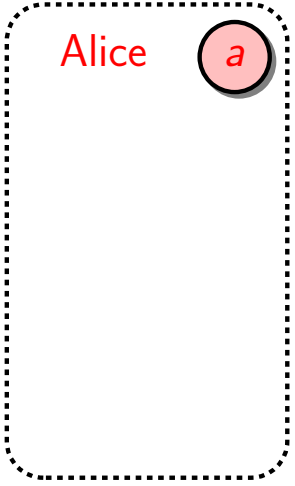

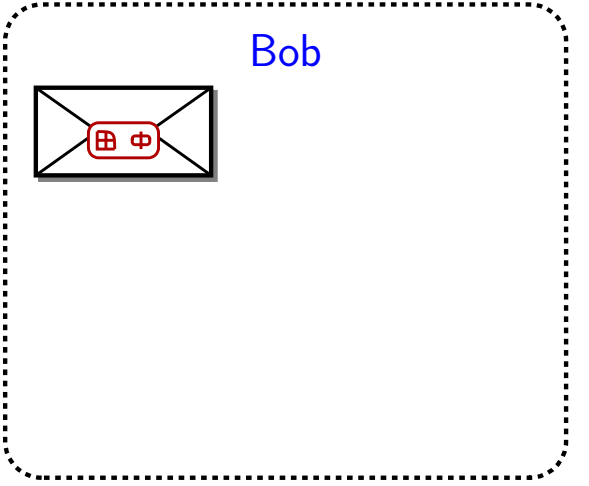

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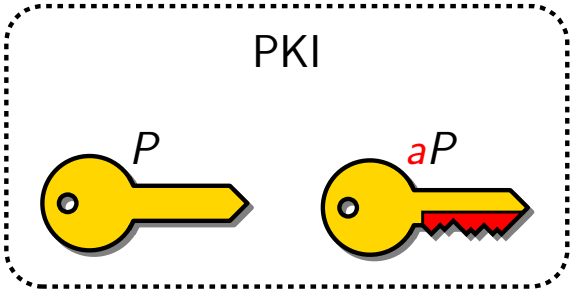

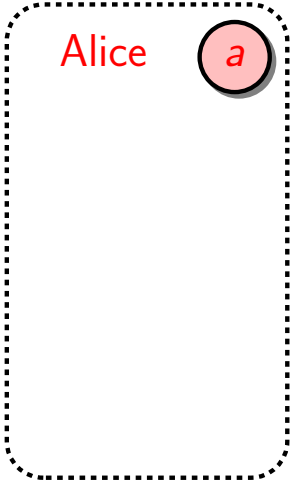

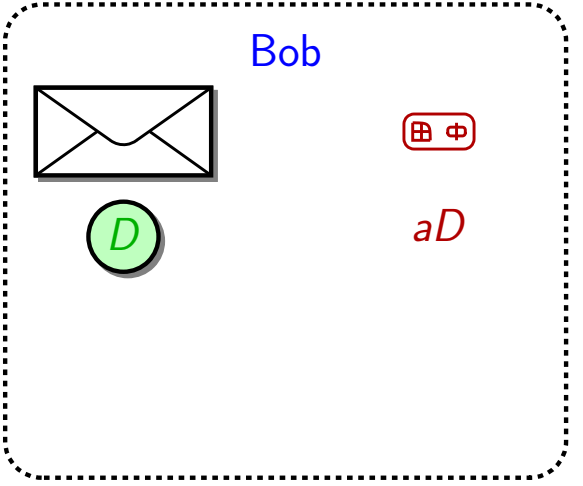

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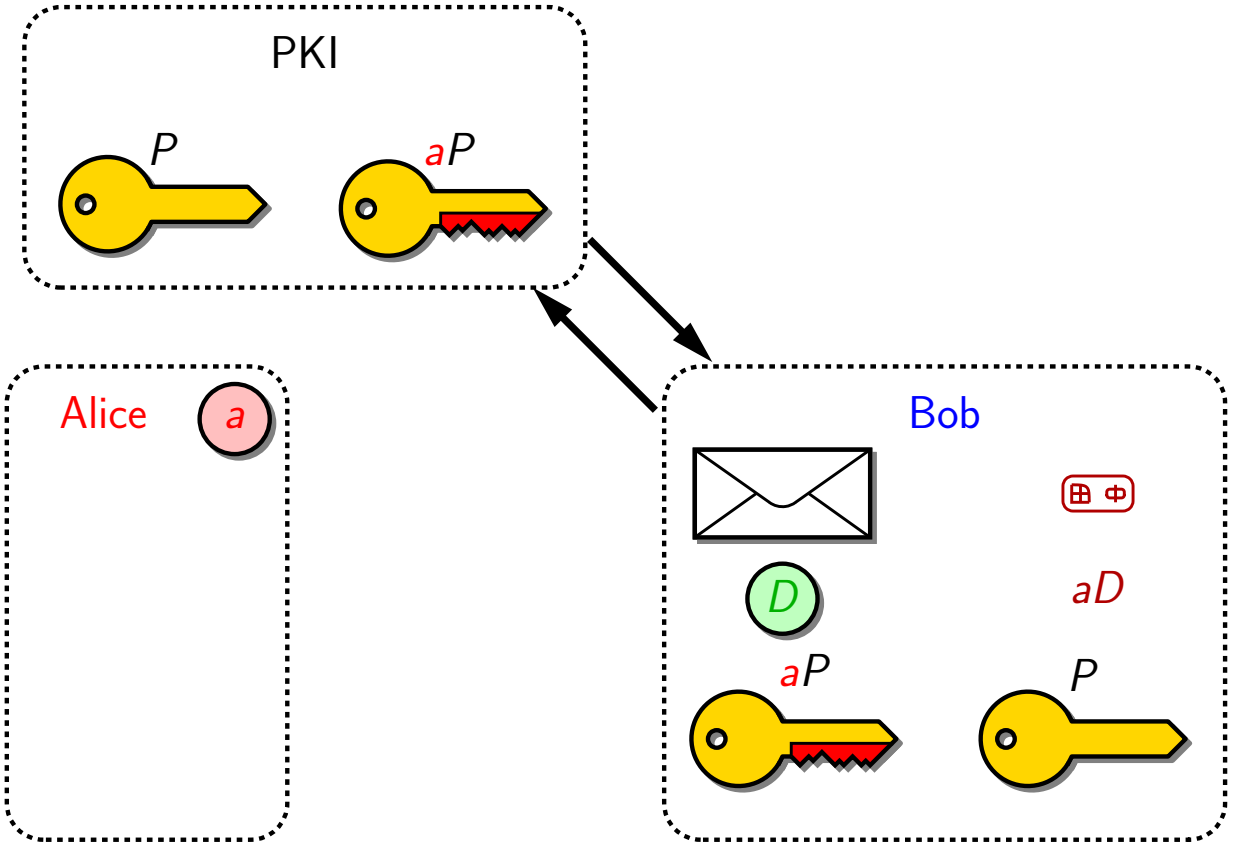

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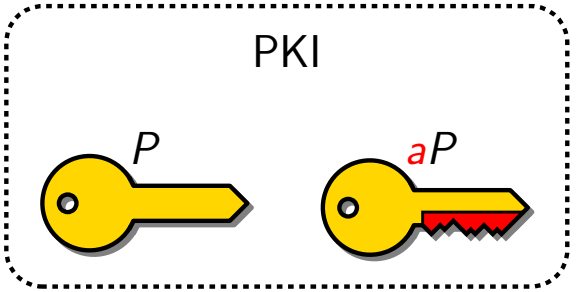

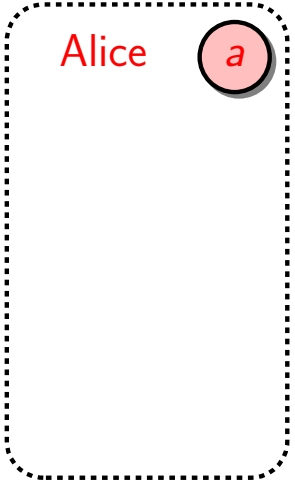

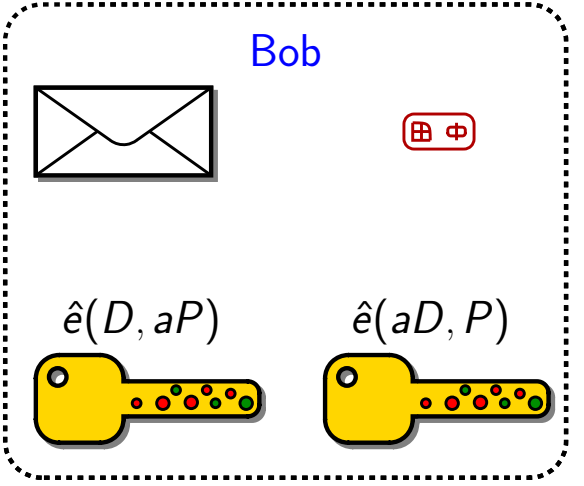

Security considerations

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- DLP should be hard on all the groups involved
- Security measurement
  - number of operations to break a cryptosystem
  - today's recommendation: 128-bit security

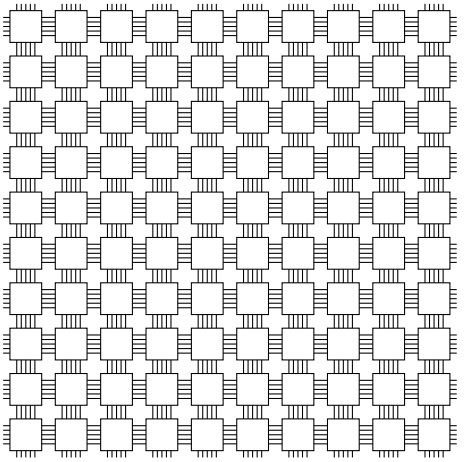
$$2^{128} \text{ operations}$$

Why cryptography and hardware implementations?

- Growth of numeric exchanges
  - many applications
    - ⋆ bank services
    - ⋆ secure firmware updates
    - ⋆ personal communications
    - ⋆ ...
  - many targets
    - ⋆ embedded electronics
    - ⋆ smart cards
    - ⋆ smartphones
    - ⋆ computers, servers
- Security implies non-trivial computations
- Need for hardware implementations
  - CPUs may be inadequate
  - limited resources

Hardware implementation

- Our target: Field Programmable Gate Array (FPGA)
  - integrated circuit
  - matrix of simple configurable logic cells
  - programmable interconnection



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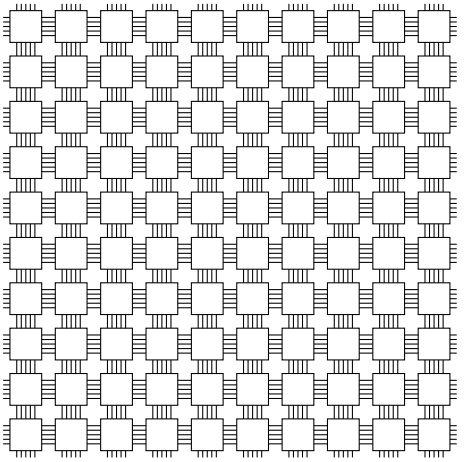

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  - time (ms)

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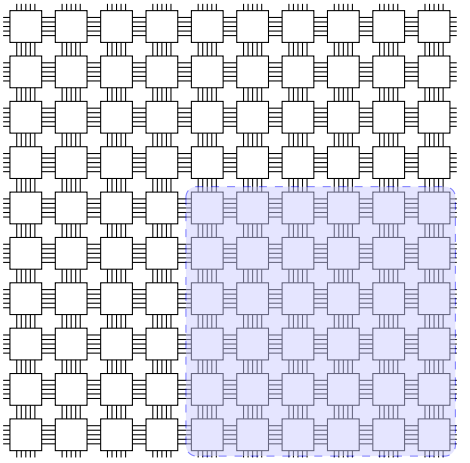

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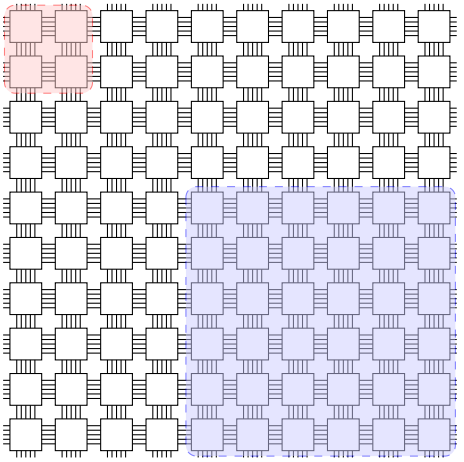

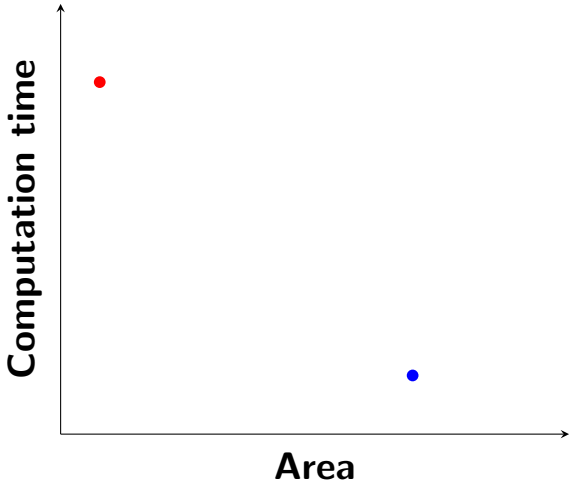

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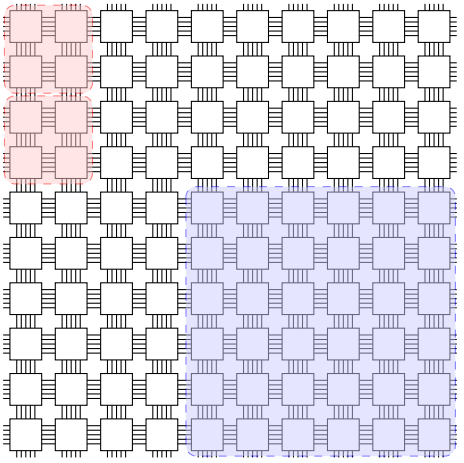

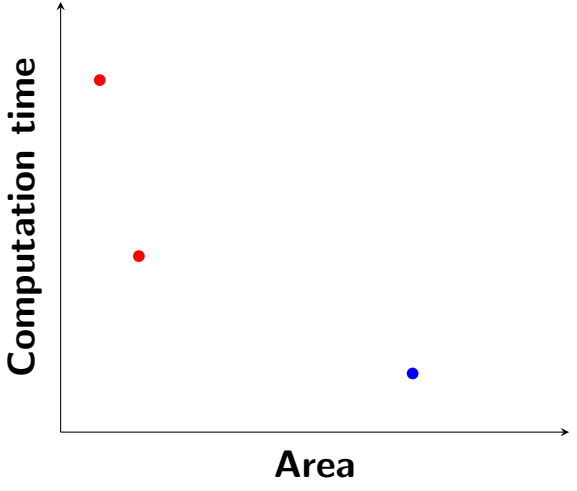

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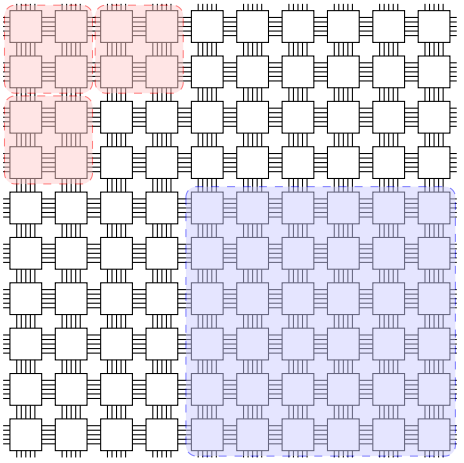

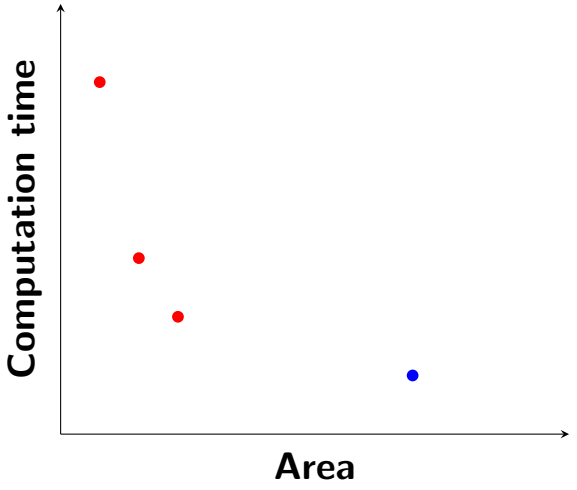

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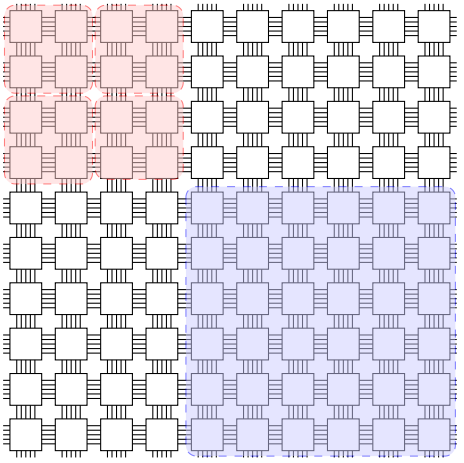

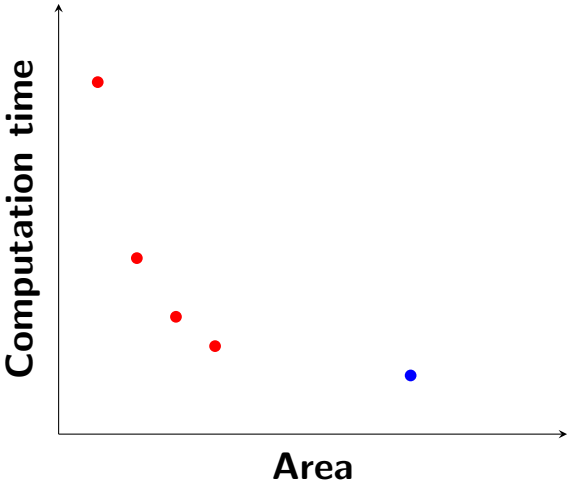

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  - time–area product
- Different designs for the same computation
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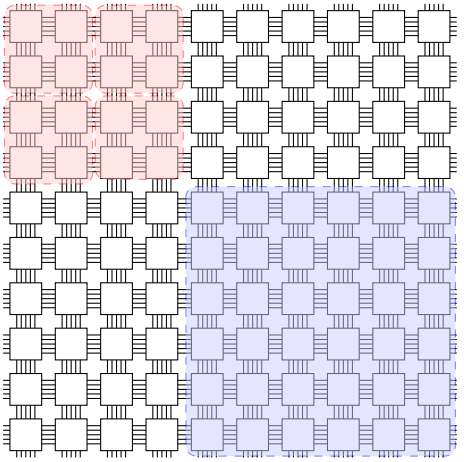

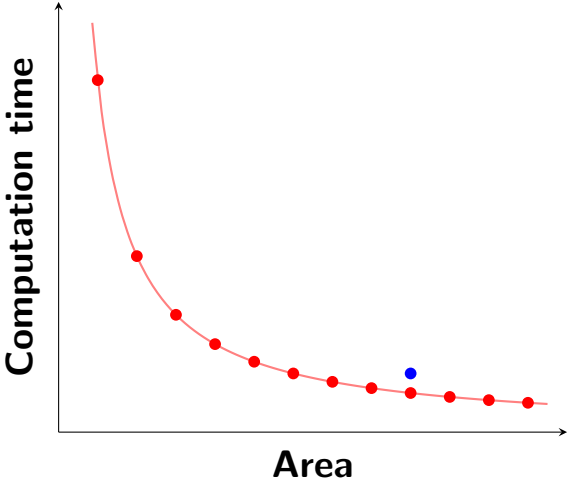

Contributions

- Fast accelerator for pairings [CHES 2009, IEEE TC 2011]
  Joint work with Beuchat, Detrey, Okamoto and Rodríguez-Henríquez
  - parallel architecture
  - pipelined subquadratic multiplier
- Compact design for pairings reaching 128-bit security
  - composite extension fields [Paring 2010]
  - hyperelliptic curves [CT-RSA 2012]
    Joint work with Aranha, Beuchat and Detrey
- Formulae for sub-quadratic multiplication [WAIFI 2012]
  Joint work with Barbulescu, Detrey and Zimmermann
  - exhaustive search
  - improved formulae for $\mathbb{F}_{3^{5m}}$

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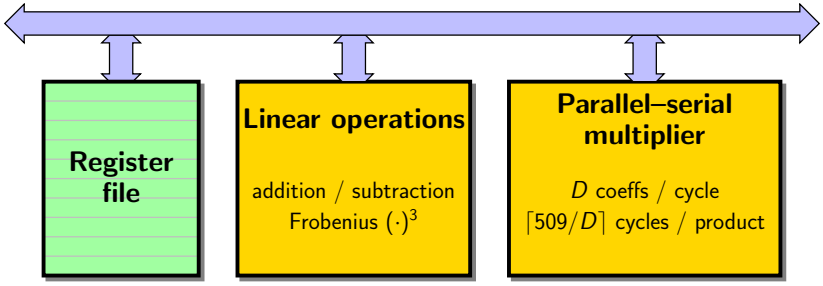
Outline of the talk

- Compact design through composite extension fields
- Pipelined subquadratic multiplier
- Conclusion and Perspectives

An arithmetic coprocessor



- For a supersingular elliptic curve over $\mathbb{F}_{3^{509}}$
- Only need arithmetic operations in $\mathbb{F}_{3^{509}}$
  - implement a specialized processor
- Multiplication is critical
  - separate linear operations and multiplications
  - careful scheduling to keep multiplier busy

Operation	count
$\times$	3638
$+$	17240
$(.)^3$	4068
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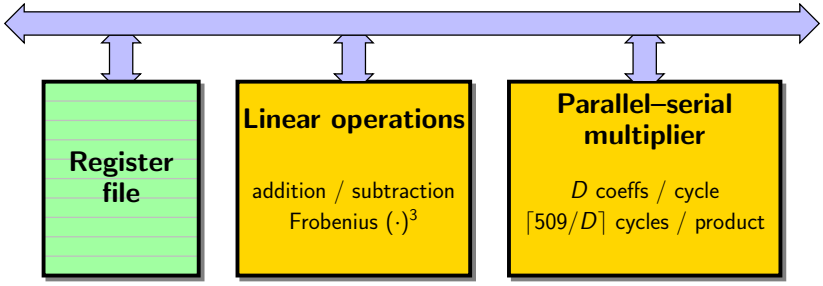

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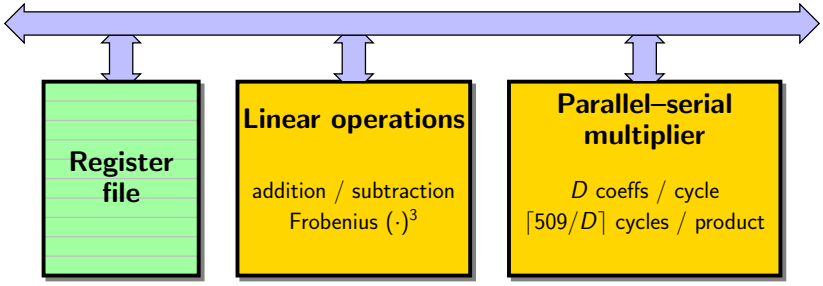

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- Inverse is only needed once: Itoh–Tsujii algorithm
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- Synthesis results for $\mathbb{F}_{3^{509}}$: 9625 slices
  - almost fully occupy a Virtex 6 LX 75 T (82%)
  - computation time: ≈ 4 ms

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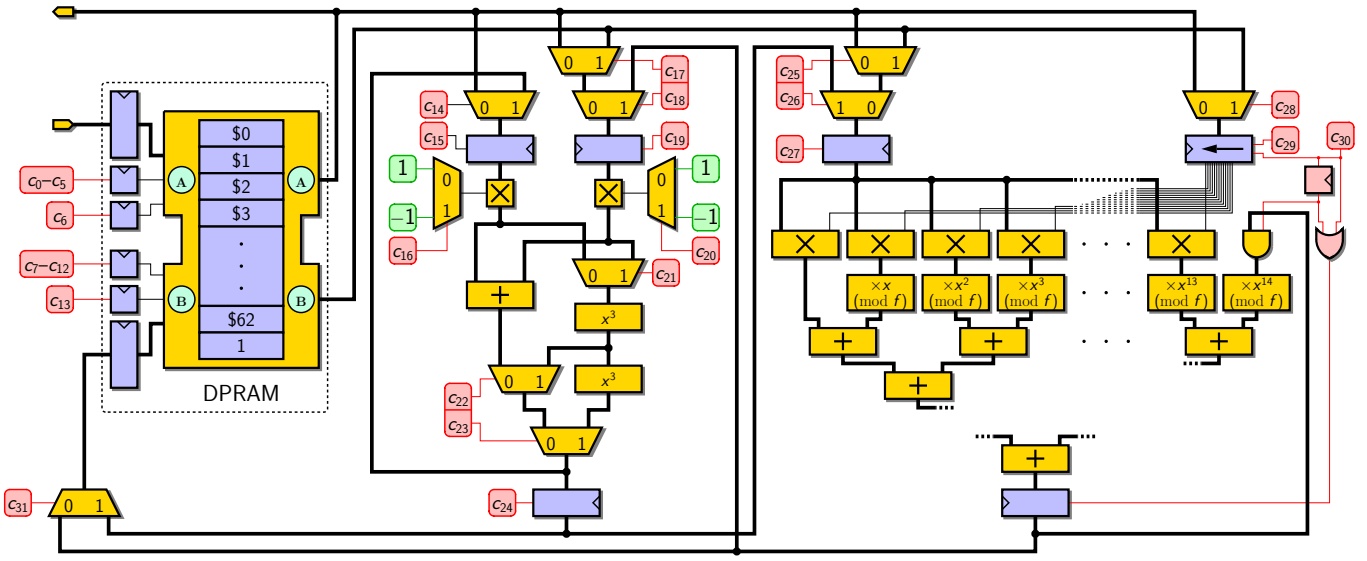
Detailed architecture of the coprocessor (char. 3)



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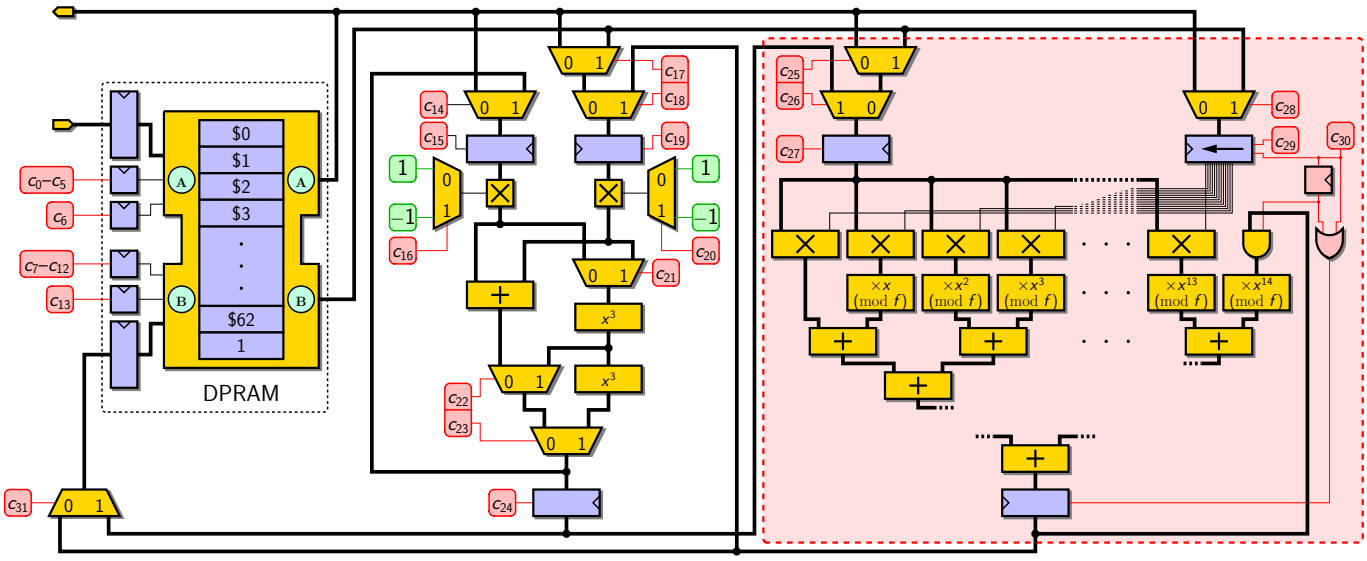

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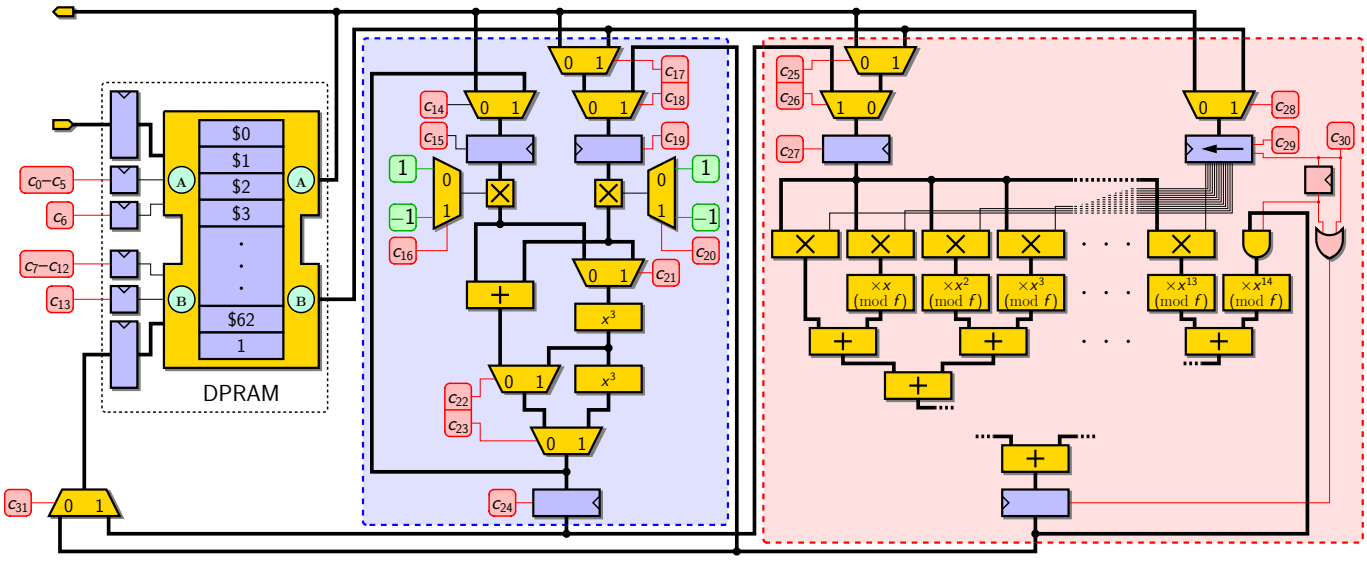

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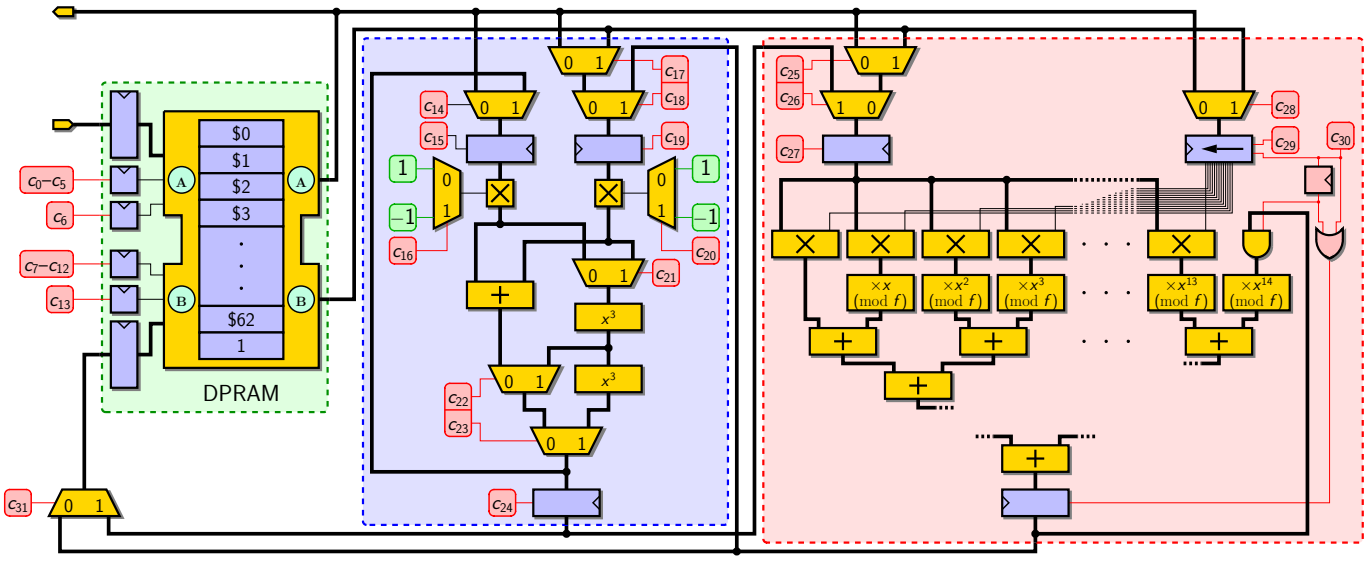
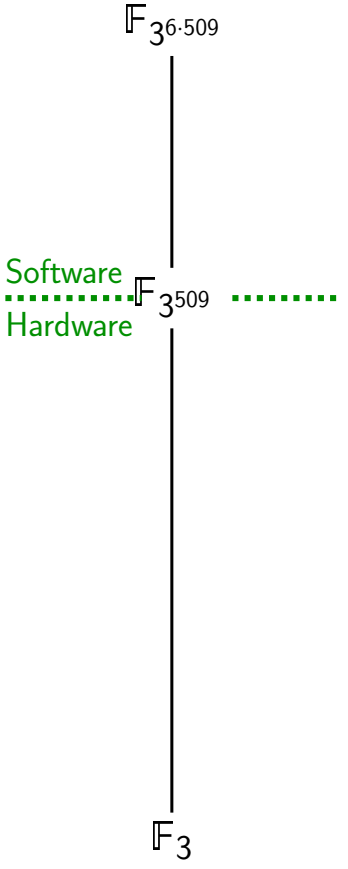
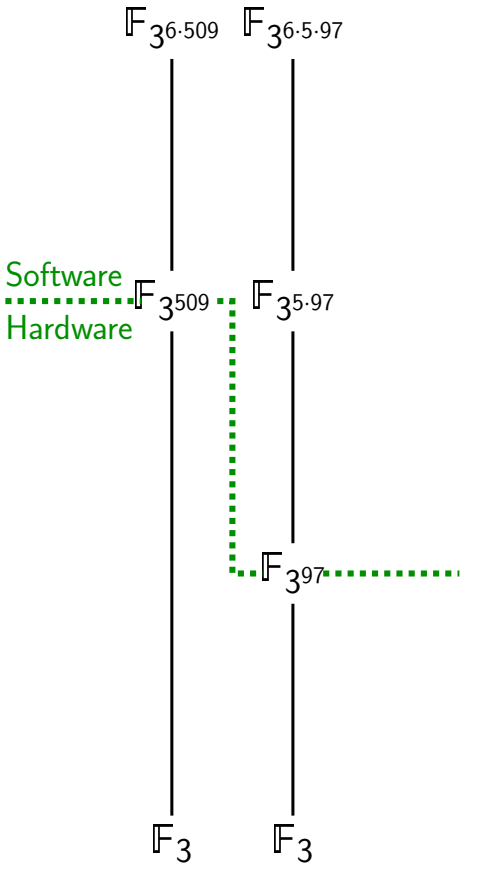


Field of composite extension degree



Field of composite extension degree

- Provides some arithmetic advantages
  - smaller datapath



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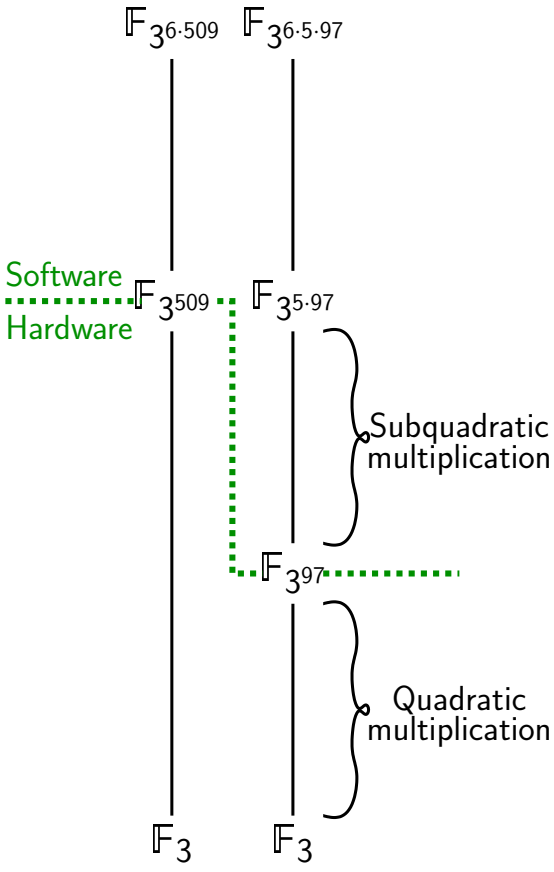

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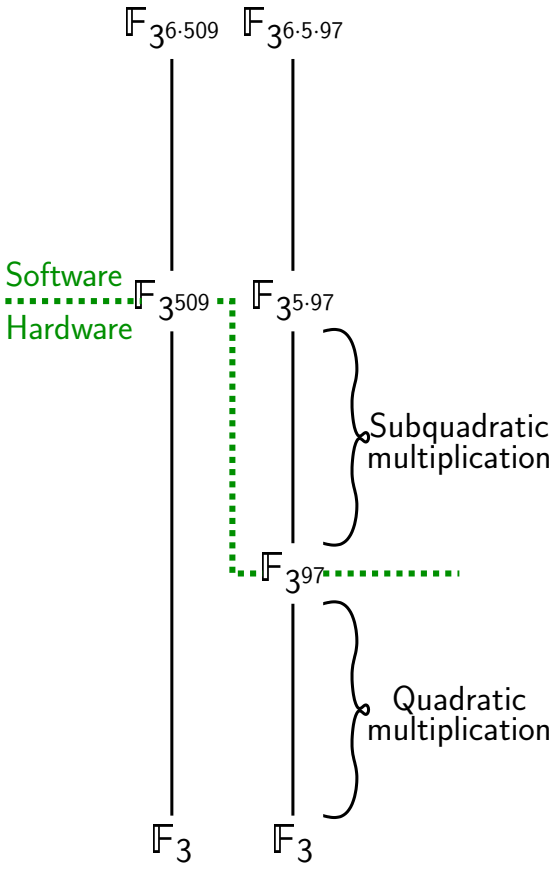

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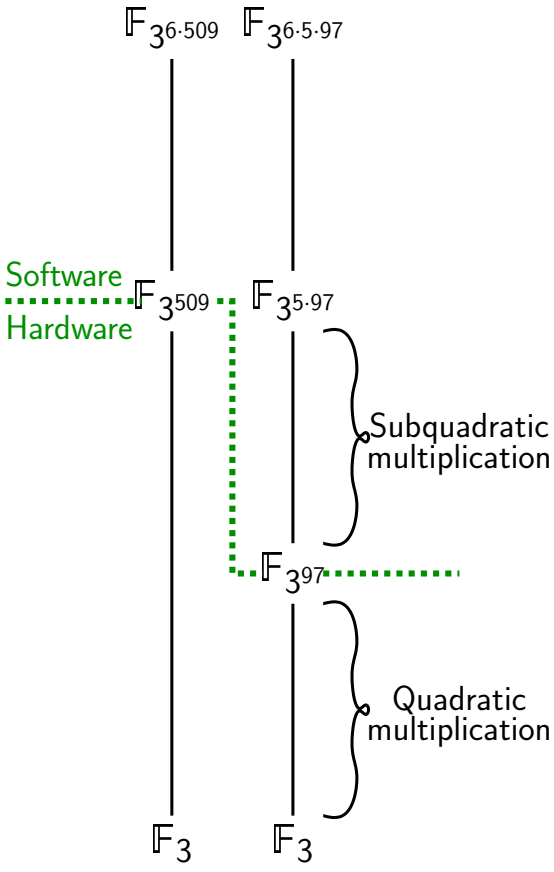
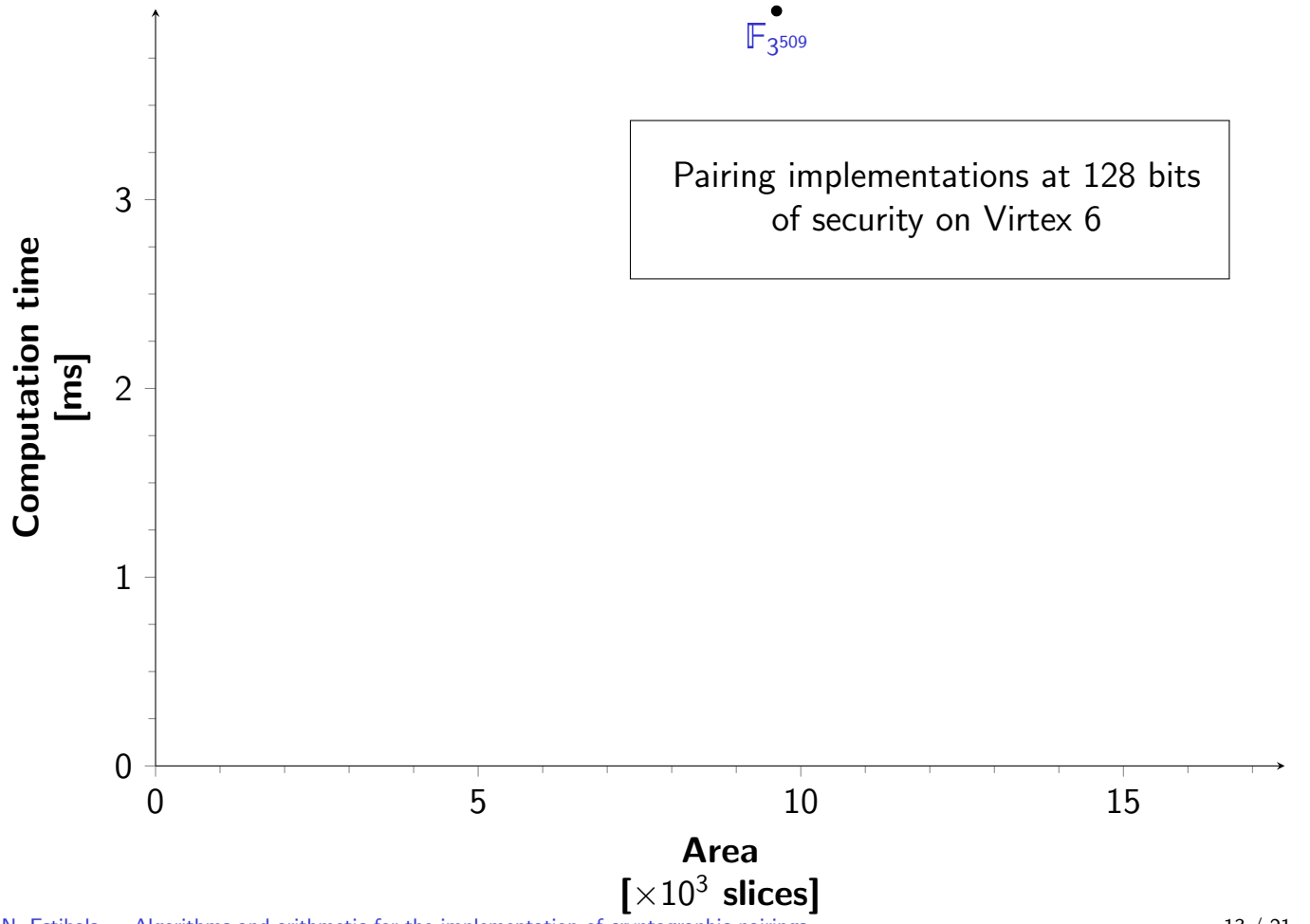
- Results
  - 1848 slices of the same Virtex 6 LX (15%)
    5.2 times smaller
  - compute a pairing in 1.6 ms
    2.5 times faster



Benchmarks


$\mathbb{F}_{3^{509}}$
Pairing implementations at 128 bits of security on Virtex 6
Computation time [ms]
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1
2
3
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5
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Area
[$\times 10^3$ slices]

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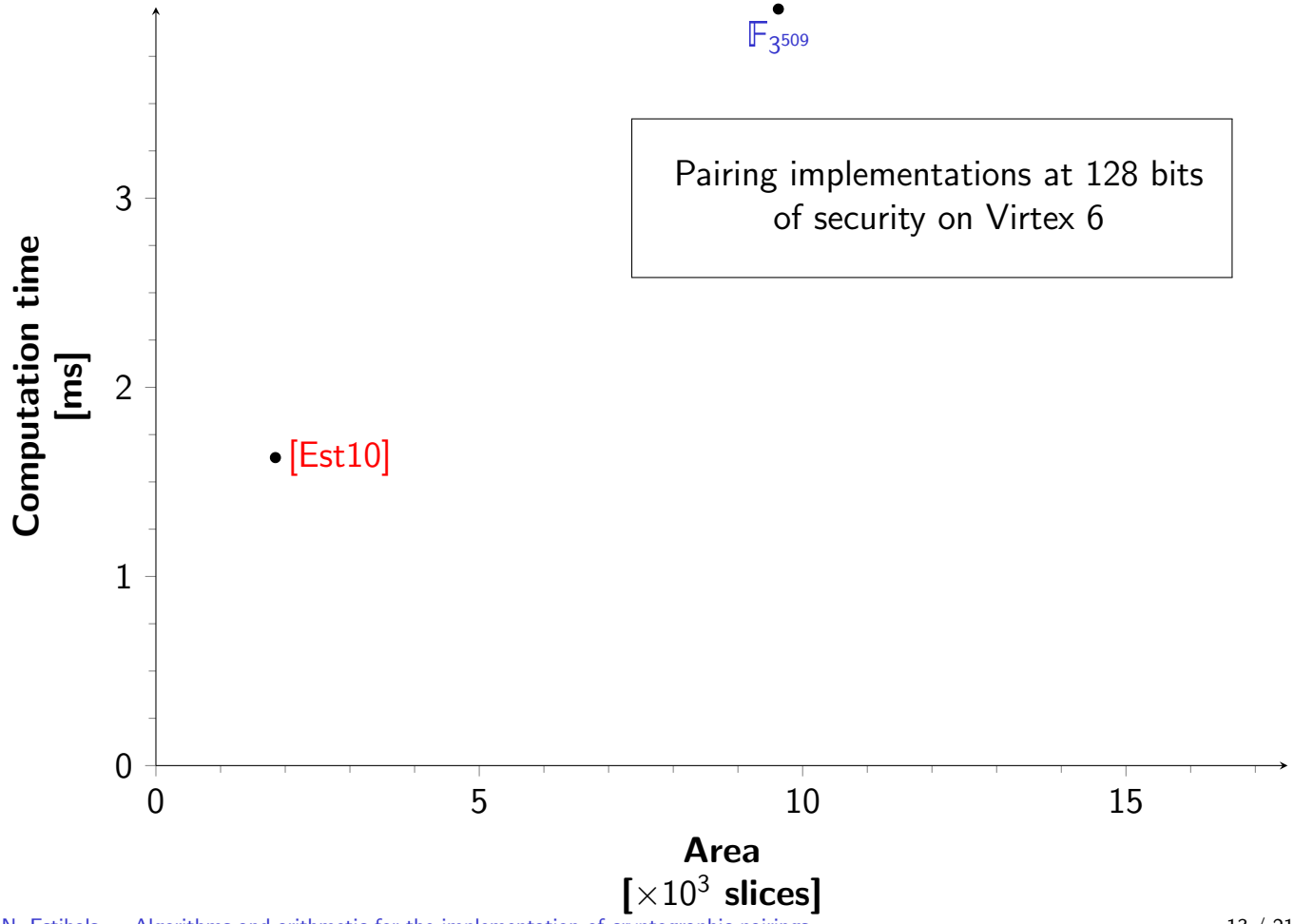
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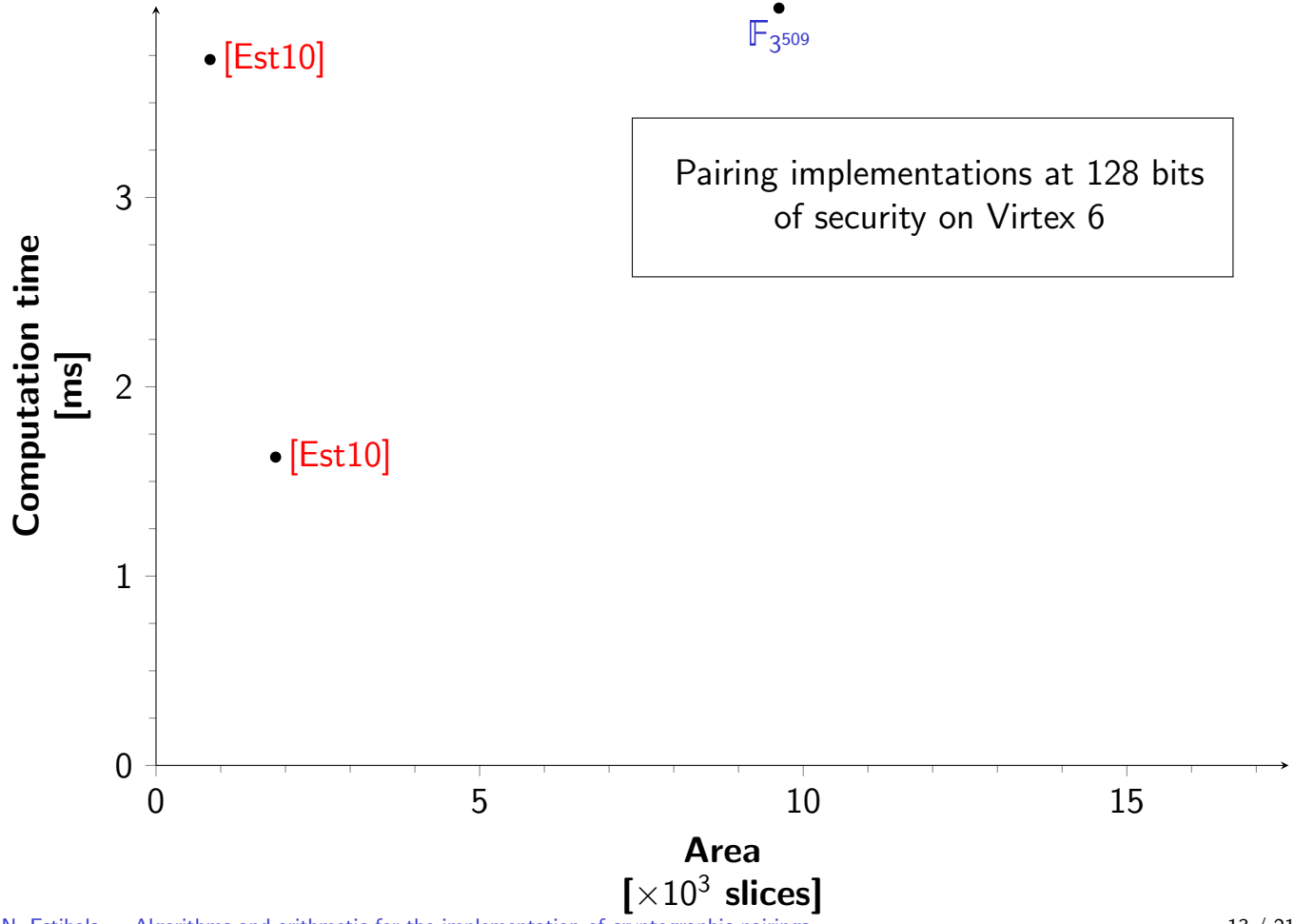
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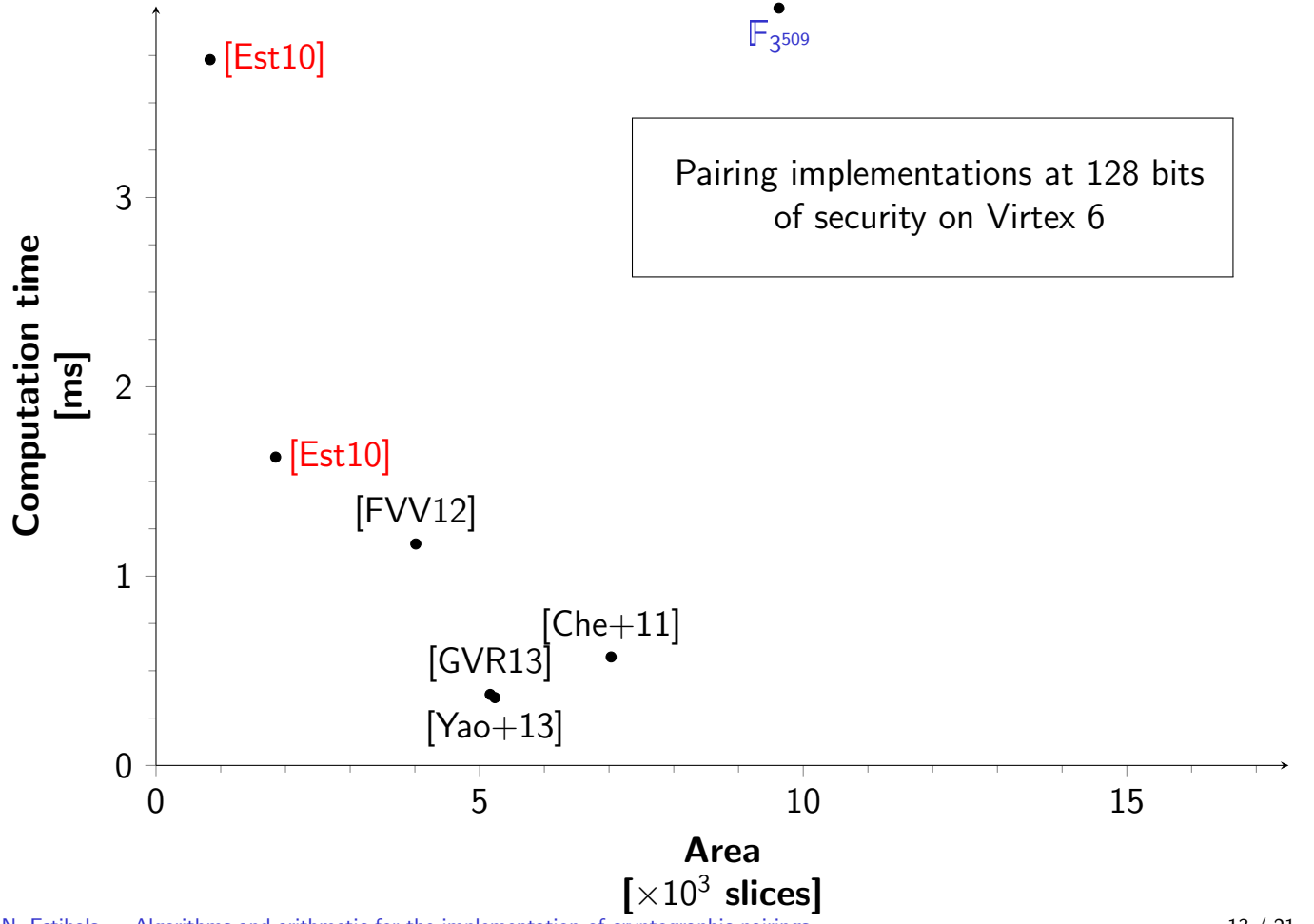
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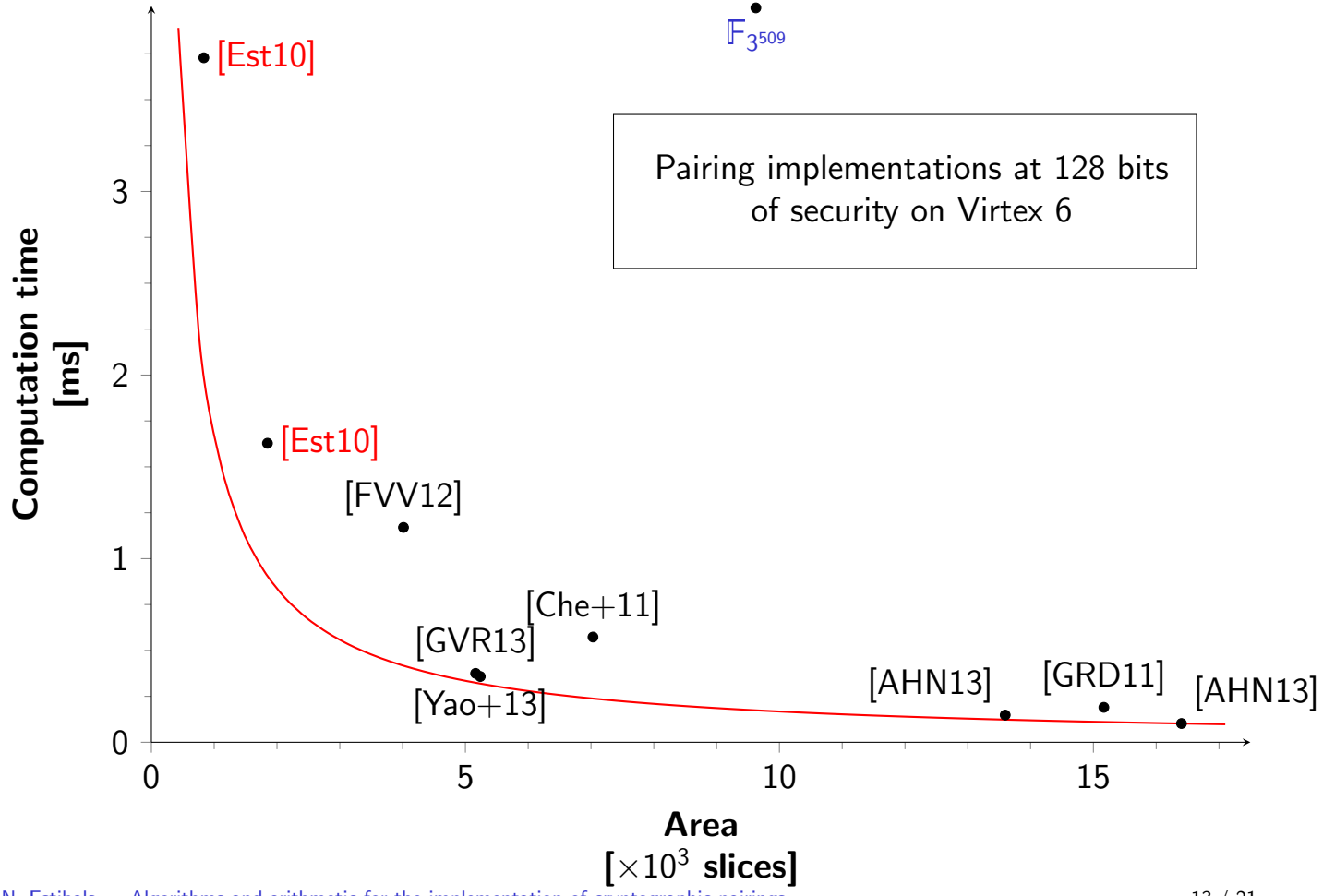
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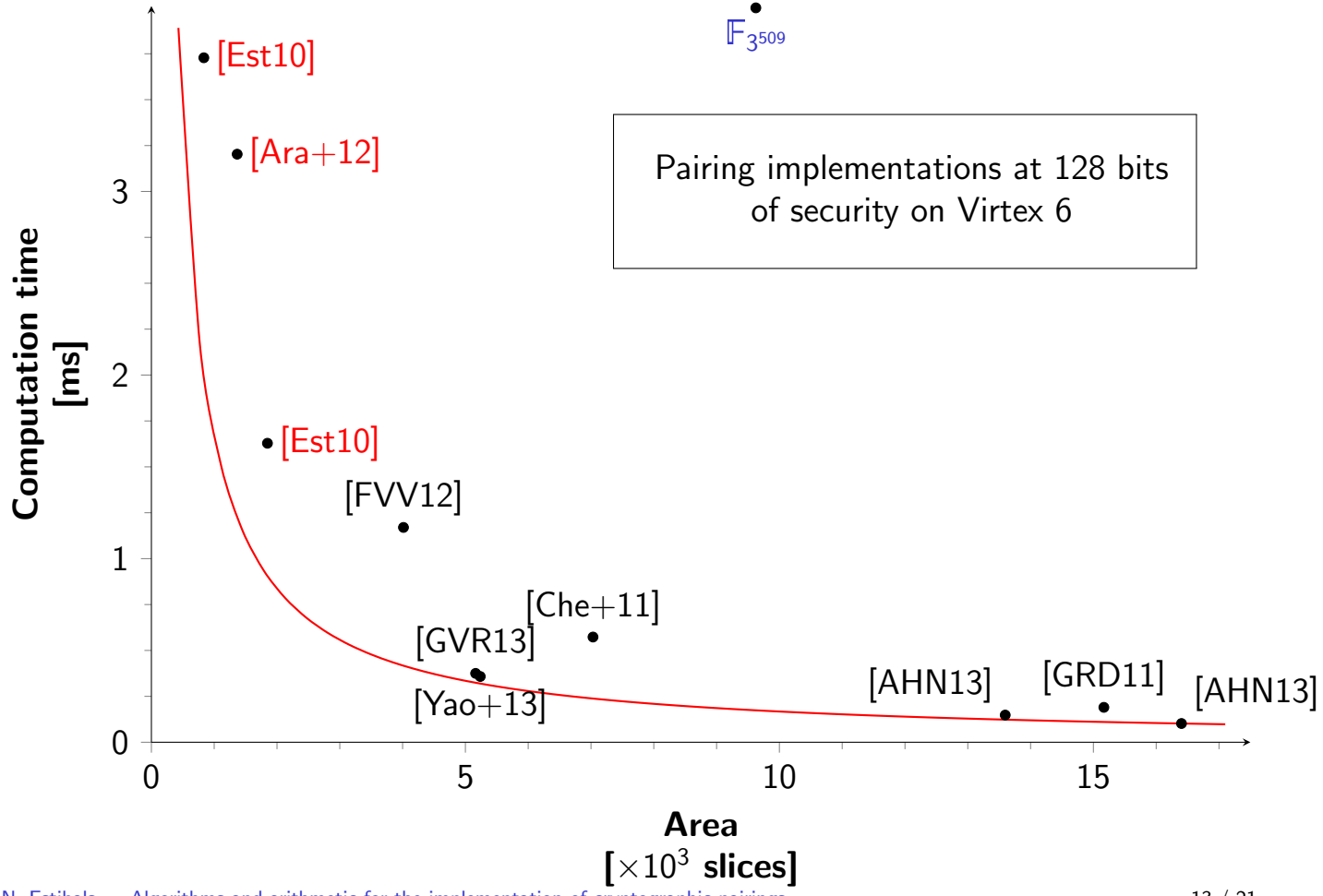
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Outline of the talk

- Compact design through composite extension fields
- Pipelined subquadratic multiplier
- Conclusion and Perspectives

Finite field representation and Karatsuba's formula

- Small characteristic fields
- Polynomial basis representation

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  - make use of fast arithmetic
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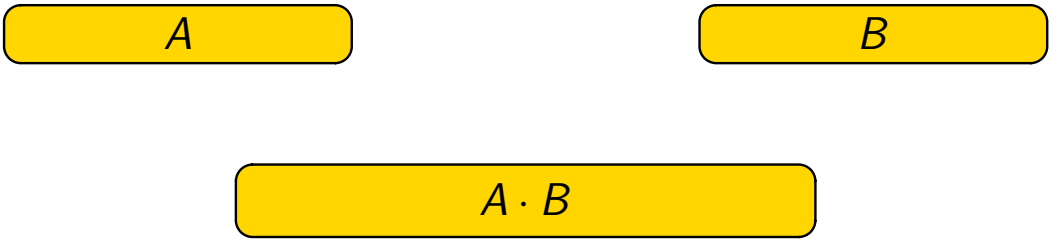

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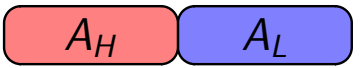

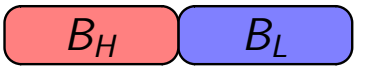

$$A_H B_H X^{2n} + (A_H B_L + A_L B_H) X^n + A_L B_L$$

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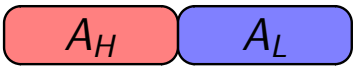

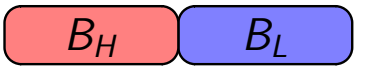

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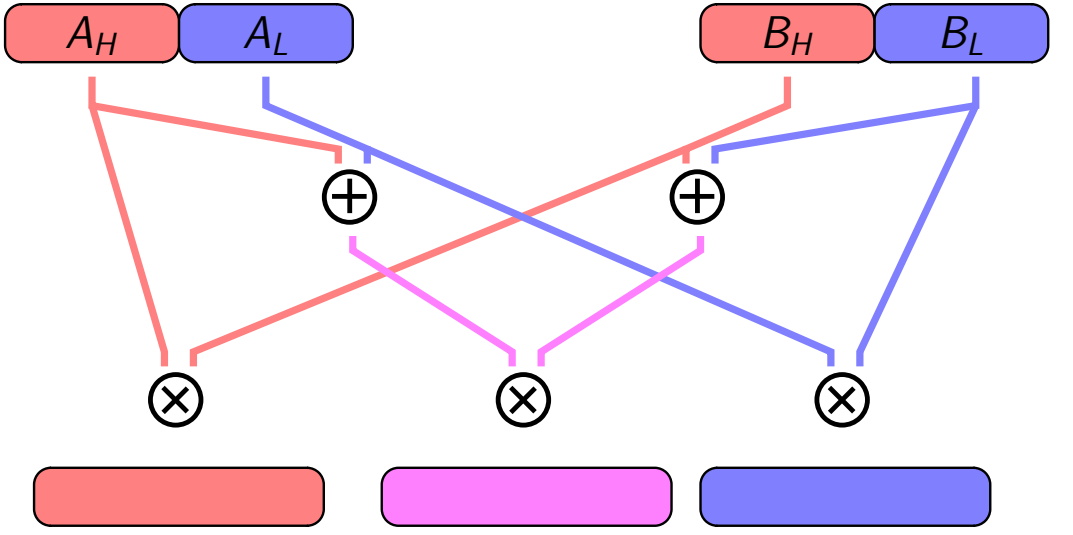

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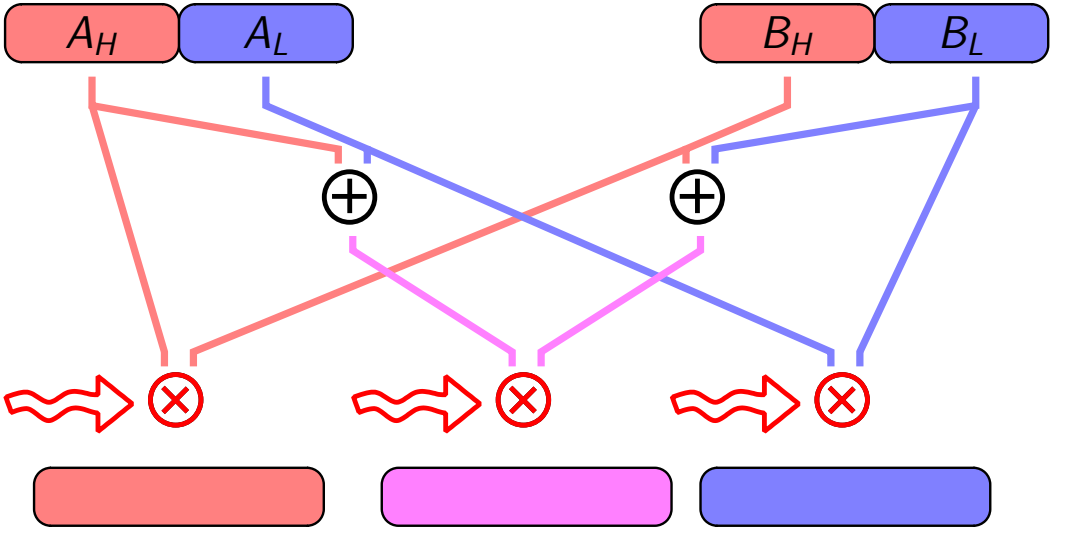

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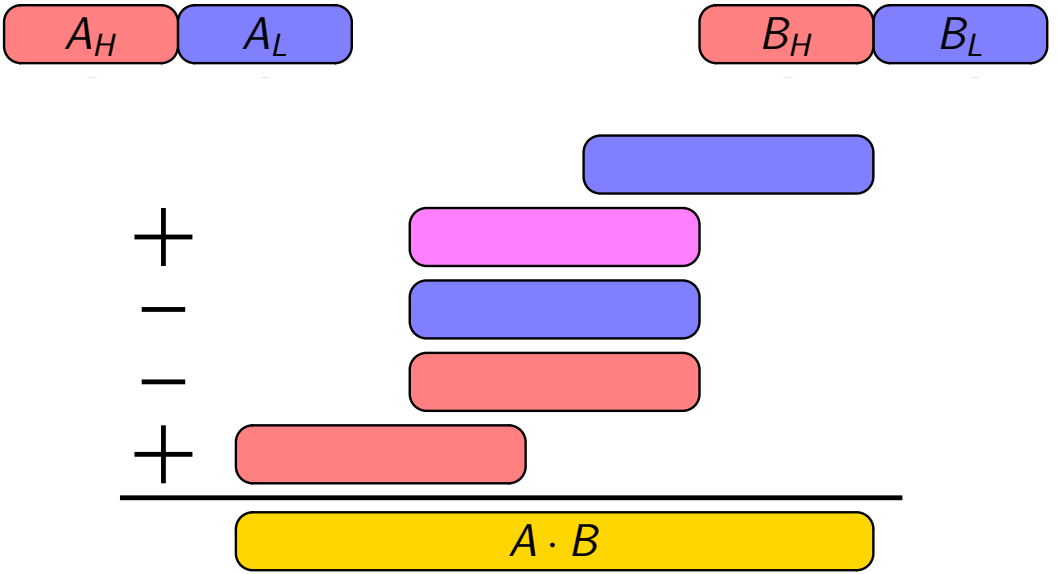
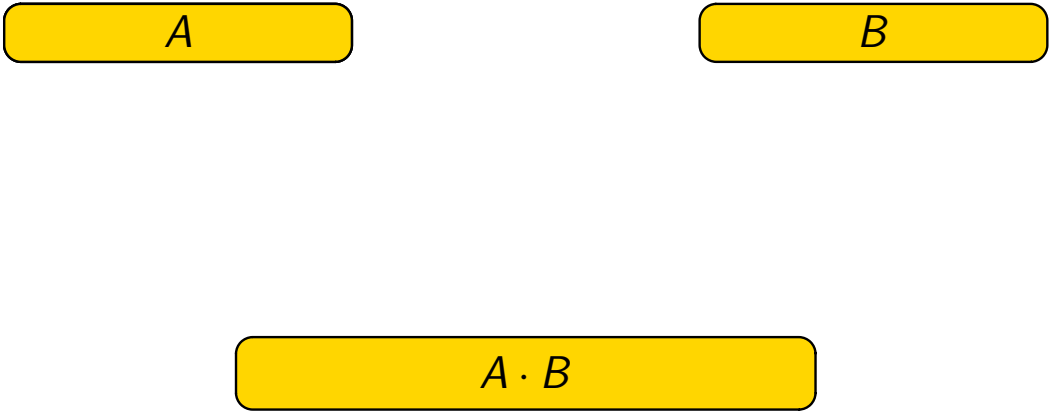


Odd–even split for Karatsuba multiplication



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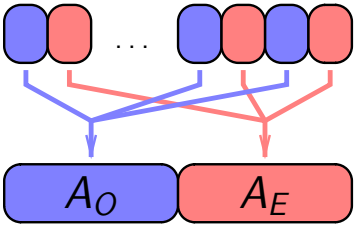

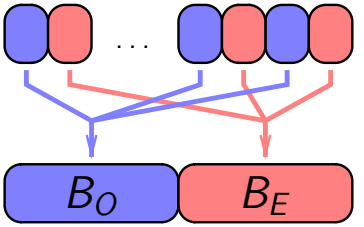

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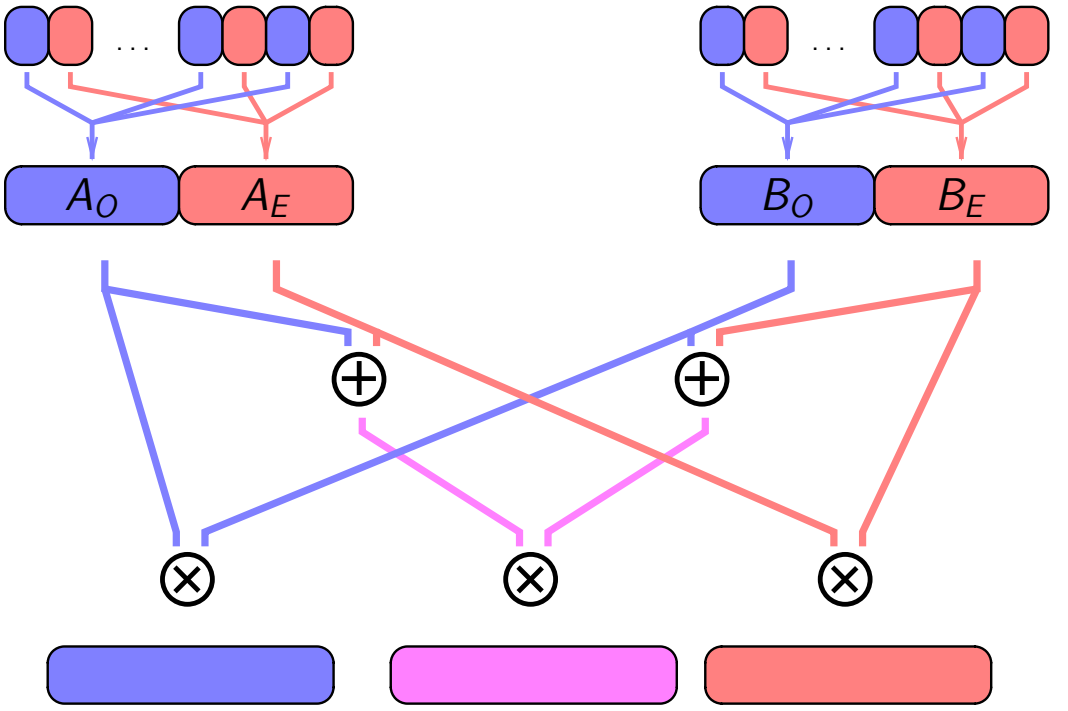

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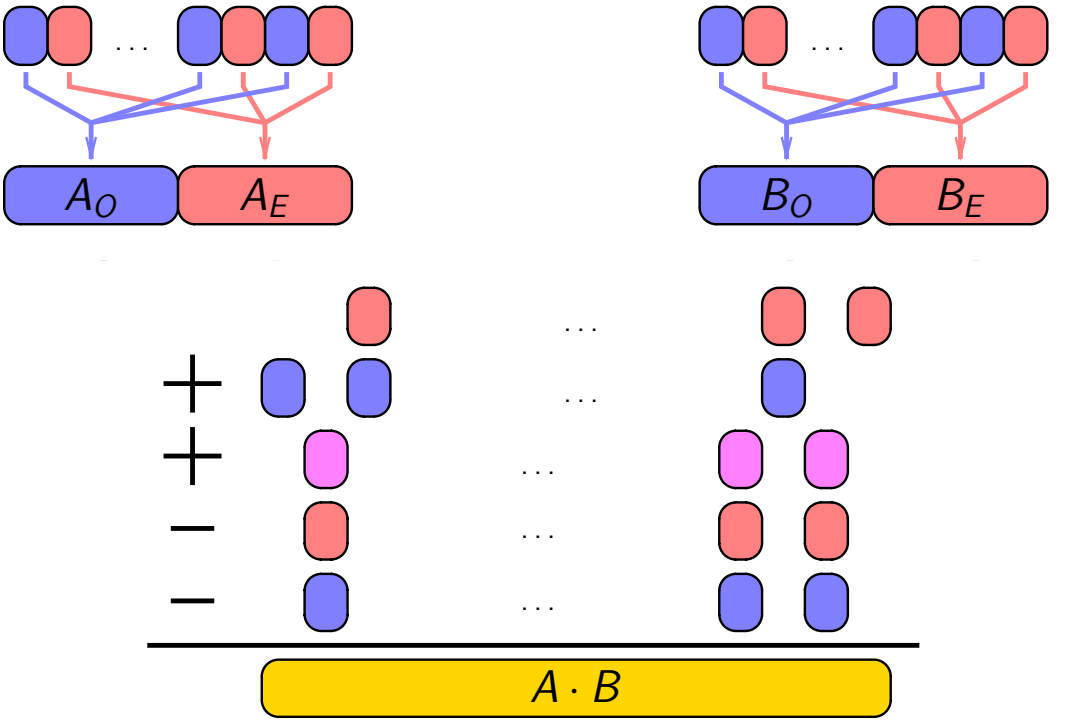

Multiplier architecture

- Karatsuba-like algorithm:
  - split the operands
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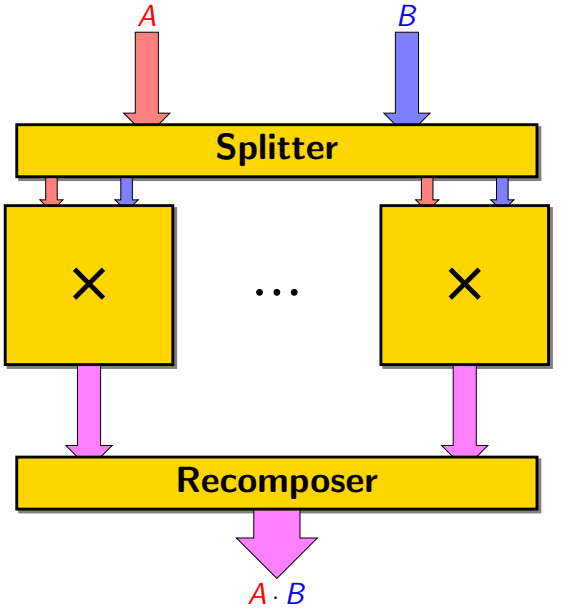
  - recompose the result
- Fully parallel evaluation of the subproducts



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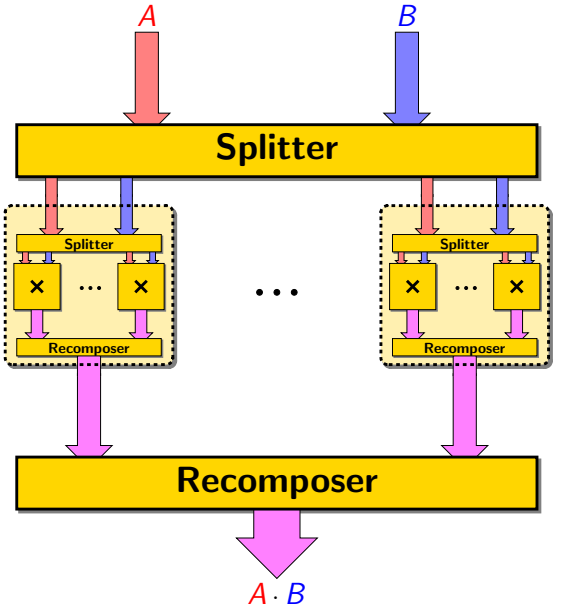

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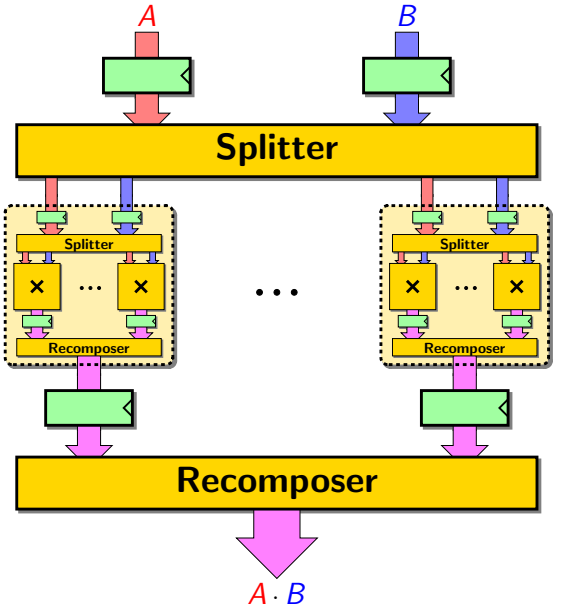

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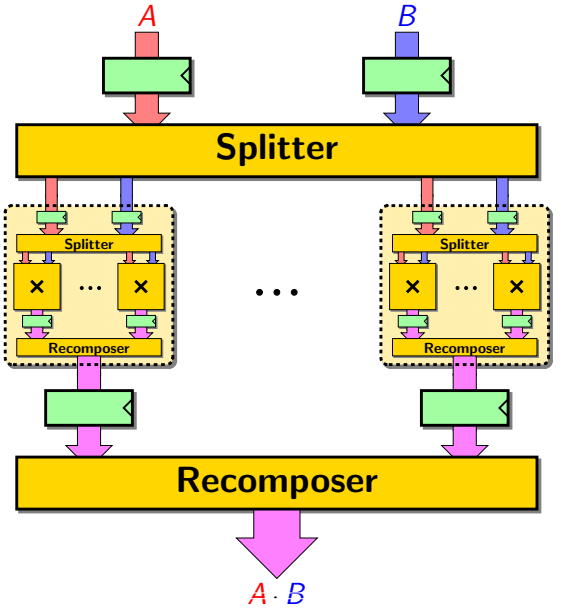
- Generated VHDL code
  - work for all small-characteristic fields
  - compare different recursions
  - configurable pipeline depth



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Conclusion

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Conclusion

- Hardware implementations of pairing
- General method for cryptographic implementations
  - study mathematical structures
  - fix parameters thanks to cryptanalysis
  - algorithmic optimizations
  - choose the right arithmetic representation
  - implement different hardware accelerators

Perspectives

- Lower-level architecture
  - FPGA is a good prototyping platform
  - but with limited uses in real-life devices
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- Use this method on different cryptographic primitives
  - scalar multiplication on hyperelliptic curves
  - lattice-based cryptography

Thank you for your attention!

Questions?