Curriculum Vitae

(Updated June 13, 2023)

Olivier Sentieys

Professor, University of Rennes 1 (Univ Rennes)
INRIA Research Chair on *Energy Efficient Computing Architectures*
ENSSAT graduate eng. school, Electronics and Computer Engineering Department
Laboratory: IRISA (UMR CNRS 6074) and INRIA Rennes - Bretagne Atlantique
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Born, April 11, 1967 in Paris, divorced, two children
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http://scholar.google.fr/citations?hl=en&user=RYvzLV8AAAAJ

1 Main current responsibilities

- Head, Taran project-team (formerly Cairn), joint team with INRIA, CNRS, University of Rennes and ENS (École Normale Supérieure) Rennes. Composed of 11 permanent academic researchers (6 Professors, 2 Ass. Prof., 3 Inria Researchers), 20 PhD students, 3 PostDoc and 5 research engineers.
- Former Head, "Computer Architecture" Department of IRISA Lab. (until Sep. 2019).
- Former Head, "Embedded Systems" branch of the SISEA (Signal, Images, Embedded Systems and Control) Master of Research (M2R) of Rennes University (until Sep. 2021).
- Recipient of Scientific Excellence Award (PEDR, PES) since 1998 without interruption.
- Leader of a French ANR project and participation to several ANR projects, and three European FP7/H2020 projects. Scientific leader of about 30 research contracts and funded collaborations.

2 Education

1999 Habilitation, University of Rennes, "Design methods for integrated circuits and embedded systems in the domain of wireless communications" (in french).

1993 PhD, University of Rennes, Signal Processing and Telecommunications, "High-level synthesis of VLSI architectures for signal and image processing: towards the design of heterogeneous multiprocessors".

1990 DEA (MSc) in Signal Processing and Telecommunications (with highest honor), University of Rennes.

1990 "Diplôme d'ingénieur", ENSSAT, Electronics and Computer Engineering Departement.

3 Professional experience

9/2002 -	Professor, University of Rennes (Univ Rennes).
9/2017 -	Holds the INRIA Research Chair on *Energy Efficient Computing Architectures*.
9/2012 - 8/2017	On secondment at INRIA Research Institute as a Senior Research Director.
9/2017	Promoted to *Exceptional Class* Professor (PRCE).
9/2008	Promoted to *First Class* Professor (PR1).
9/2007 - 2012	On leave (half time) at INRIA Research Institute.
9/2001 - 8/2002	Full-time researcher at INRIA/IRISA Rennes.
9/1994 - 8/2001	Associate Professor, University of Rennes I.
2003 - 2009	Invited Professor several times at Laval University, Canada, total of 3 months.
9/2010	Invited Professor, University of Massachusetts, Amherst, USA, 2 weeks.
9/2012	Invited Professor, University of Sherbrooke and University of Quebec, Canada, 1 month.

4 Main scientific and teaching responsibilities

6/2010 - 9/2019	Head, "Computer Architecture" Department of IRISA Lab.
1/2008 -	Scientific leader of TARAN project-team at IRISA/INRIA (35 people).
5/2002 - 12/2007	Scientific co-leader of R2D2 team at IRISA (30 people).
9/1996 - 4/2002	Scientific leader of Signal - Architecture team of the LASTI Lab. (20 people).
2001 -	Head, "Embedded Systems" branch of the SISEA (Signal, Images, Embedded Systems and Control) Master of Research (M2R) of Rennes University.
9/1999 - 9/2001	Head, electronics engineering department at ENSSAT.
1996 -	Scientific leader of about 30 research contracts and funded collaborations.
2002	Co-founder of Aphycare technologies, a company developing embedded sensors for biomedical applications and elderly person surveillance.

5 Research activities

My research activities are in the complementary fields of computer architecture, computer arithmetic, embedded systems and signal processing. Roughly, I work firstly on the definition of new system-on-chip architectures, especially the paradigm of reconfigurable hardware accelerators, and their associated CAD tools, and secondly on some aspects of signal processing like finite arithmetic effects and digital communications. For more information, see the activity reports of the TARAN team or my web page.

Recent research themes:

- Hardware acceleration for signal, image, machine learning, deep learning and data mining.
- Approximate computing, automatic floating-point to fixed-point conversion, analytical accuracy evaluation, customized arithmetic.
- Energy efficiency, fault-tolerance, and security of computing architectures.
- Reconfigurable systems, coarse-grain/fine-grain reconfigurable architectures, runtime reconfiguration, embedded FPGA.
- Optical and wireless network on chip.
- System-level design of hardware accelerators and system-on-chip architectures.
- Ultra-low-power architectures for wireless sensor networks (WSN), energy-harvesting WSNs.

Software and Hardware Developed

- **TypEx** (Type Exploration) is a tool designed to automatically determine custom number representations and word-lengths (i.e., bit-width) for FPGAs and ASIC designs at the C source level. The main goal of TypEx is to explore the design space spanned by possible number formats in the context of High-Level Synthesis. TypEx takes a C code written using floating-point datatypes specifying the application to be explored. The tool also takes as inputs a cost model as well as some user constraints and generates a C code where the floating-point datatypes are replaced by the wordlengths found after exploration. The best set of word-lengths is the one found by the tool that respects the given accuracy constraint and that minimizes a parametrized cost function. TypEx is currently used by Huwaei for optimizing its phone camera chips and is the basis of a future start-up, currently in incubation, to be created in 2020. https://gitlab.inria.fr/gecos/gecos-float2fix.
- **Comet** is a RISC-V pipelined processor with data/instruction caches, fully developed using High-Level Synthesis. The behavior of the core is defined in a small C code which is then fed into a HLS tool to generate the RTL representation. Thanks to this design flow, the C description can be used as a fast and cycle-accurate simulator, which behaves exactly like the final hardware. Moreover, modifications in the core can be done easily at the C level. https://gitlab.inria.fr/srokicki/Comet
- **ID.Fix** is an infrastructure for the automatic transformation of software code aiming at the conversion of floating-point data types into a fixed-point representation. http://idfix.gforge.inria.fr.
- **Zyggie** is an autonomous Wireless Body Sensor Network (WBSN) platform to monitor, analyze, and classify body movements. Zyggie is composed of a processor, a radio transceiver, an UWB centimeter ranging, and different sensors including an Inertial Measurement Unit (IMU) with 3-axis accelerometer, gyrometer, and magnetometer. Zyggie is used for evaluating data fusion algorithms, low power computing algorithms, wireless protocols, and body channel characterization in the BoWI project funded by CominLabs. https://bowi.cominlabs.u-bretagneloire.fr/zyggie-wbsn-platform
- **SmartSense** is a sensor network platform for smart building research collecting several data related to energy consumed and uses in buildings. Each node comprises several sensors: camera, infra-red, audio, radio spectrum sensing, 9-axis inertial, humidity, atmospheric pressure, temperature, light (RGBW, UVA, UVB), centimeter precision distance ranging, C02+VOC. With more than 200 nodes deployed at Inria (Lannion and Rennes), SmartSense provides data for applications in data mining, electrical load disaggregation or in sensor processing. Taran studies sensor-aided Non-Intrusive Load Monitoring (NILM) [RVS19] where a small number of autonomous sensors can help disaggregation algorithms to detect and identify the power consumption of the operating devices from a single meter on the main power line. http://smartsense.inria.fr/
- **PowWow** (Power Optimized Hardware and Software FrameWork for Wireless Motes) is a hardware and software platform designed to handle wireless sensor network (WSN) protocols and related applications. Based on our MAC protocol and other innovating features, PowWow results in a very light memory usage and in 15x less power consumption than the equivalent ZigBee standard. http://powwow.gforge.inria.fr.
- **Ochre** (On-Chip Randomness Extraction) is a set of synthesizable IP models for true- and pseudo-random number generation and hardware accelerated statistical tests. It includes IP cores of different oscillator-based TRNGs, different PRNGs (linear feedback shift registers, cellular automata, AES-based) and several statistical tests (FIPS 140-1 and AIS31). This set of IPs has been used to design two version of the Ochre chip.
- As a proof of concept of our power-gated hardware task approach, a chip has been designed and fabricated in a 65nm CMOS from STMicroelectronics.

Keywords: Embedded System Design, System-on-Chip, Reconfigurable Hardware Accelerators, Low-Power and Energy Efficiency, Approximate Computing, Finite Arithmetic Effects, Signal Processing for Wireless Communications, Wireless Sensor Networks.

Publications: 4600 citations, h-index=35. Complete list: http://people.rennes.inria.fr/Olivier.Sentieys/?page_id=2
Google Scholar: http://scholar.google.fr/citations?hl=en&user=RYvzLV8AAAAJ.

6 Leadership within the Scientific Community

- Elected member of the Evaluation Committee (CE) of INRIA since 2019.
- Member of the IEEE/ACM DATE Executive Committee (DEC) since 2022.
- Jury member in the EDAA (European Design and Automation Association) Outstanding Dissertations Award (ODA) delivered during DATE Conference since 2016.
- Member of the committee for delivering the Best Paper Award at IEEE/ACM DATE 2020 and 2022.

- Member of the ANR Scientific Evaluation Committee CE25 "Software science and engineering - Multi-purpose communication networks, high-performance infrastructure".

- Member of the French National University Council (CNU section 61) from 1999 to 2007.
- Member of the ANR ARPEGE evaluation committee (2010).
- Member of AERES evaluation committee for research laboratories.
- O. Sentieys is a member of the "Allistene" alliance between INRIA, CNRS and CEA, Working Group on software systems since 2010.
- Expert for Natural Sciences and Engineering Research Council of Canada (NSERC), ANVAR, Region Rhône-Alpes, Region Languedoc and fonds québécois de la recherche sur la nature et les technologies (FQNRT).
- Expert for ANR and CNRS (blanc, jc, redoc, arpege, cosinus, PEPS).
- Expert for *Primes d'Excellence Scientifique* (PES) in 2009.

- Chair of the IEEE Circuits and Systems (CAS) French Chapter (2004-2014).
- Member of the Steering Committee of the SOC2 Expert Group at the CNRS and of the GDR SOC2.
- Member of the Steering Committee of GRETSI.
- Member of IEEE and ACM.

7 Program committees, editorial boards, conference organization

- Journal editorial board member of: Journal of Low Power Electronics (since 2006), International Journal of Distributed Sensor Networks (2011–2018).
- Technical Program Committee member of:
  - IEEE/ACM Design and Test in Europe (DATE), 2011–2014, 2016–2022.
  - Co-Chair of the Track on Architectural and Microarchitectural Design at IEEE/ACM DATE (2018–2020).
  - Chair of the Track on Architectural and Microarchitectural Design at IEEE/ACM DATE (2020–2022).
  - International Conference on Field Programmable Logic and Applications (FPL), 2013–.
  - IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2014, 2023.
  - ACM Symposium on Integrated Circuits and Systems Design (SBCCI), 2010–.
  - Track Chair, IEEE Northeast Workshop on Circuits and Systems (NEWCAS), 2009–2018.
  - ACM Int. Work. on Energy Neutral Sensing Syst. (ENSSys), co-located with ACM SenSys, 2013–.
  - International Conference on Cognitive Radio Oriented Wireless Networks (CROWNCOM), 2016.
  - International Conference on ReConFigurable Computing and FPGAs (ReConFig), 2016–.

Awards, Invited Talks, and Summer Schools

- Davide Pala received the A. Richard Newton Young Fellow Award at IEEE/ACM Design Automation Conference (DAC), San Francisco, 2018.

- *Best Paper Award*, IEEE Comp. Soc. Annual Symp. on VLSI (ISVLSI), 2013 "Energy-Aware Computing via Adaptive Precision under Performance Constraints in OFDM Wireless Receivers" F. Cladera, M. Gautier, O. Sentieys.
- The paper "A polynomial time algorithm for solving the word-length optimization problem" was nominated as *Best Paper Award*, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2013.
- *Best Student Paper Award*, IEEE INMIC'09, "Toward Ultra Low-Power Hardware Specialization of a Wireless Sensor Network Node" A. Pasha, S. Derrien and O. Sentieys.

Invited Talks

- Keynote at the IEEE International Nanodevices and Computing (INC) - IEEE International Conference on Rebooting Computing (ICRC), Grenoble, France, April 2019 on "Playing with numbers for Energy Efficiency: Introduction to Approximate Computing" [Sen19].
- Keynote at the Third Workshop on Approximate Computing (AxC), in conjunction with IEEE European Test Symposium (ETS), Bremen, Germany, June 2018 on "Playing with number representations and operator-level approximations" [Sen18].
- Keynote at the Journées Scientifiques Inria (JSI) on "Opportunities for computer architecture research with open-source hardware - The case of RISC-V", Nov. 2022.
- Invited talk at HiPEAC Computing Systems Week (CSW), Lyon, France, Oct 1, 2021 on "Approximate Deep Learning Accelerators: Improving performance and energy efficiency of deep-learning hardware accelerators with controlled arithmetic approximations" [Sen21a].
- Invited talk at Dagstuhl Seminar 21302 - Approximate Systems on "An Optimization Playground for Precision and Number Representation Tuning" [Sen21b].
- Invited talk at IIT Goa, India on "An Optimization Playground for Precision and Number Representation Tuning".
- Invited talk at "Séminaire sur la Tolérance Aux Fautes des Equipements Electroniques pour la Defense" (STAFEED) on "vulnerability analysis of embedded digital systems: from physics to micro-architecture".
- Invited talk at IoT2Sustain Workshop, London, UK, July 2017 on "Challenges in Energy Efficiency of Computing Architectures: from Sensors to Clouds".
- Other Invited Talks and Keynotes in Conferences and Workshops: FPL'14 (workshop on self-adaptive heterogeneous many-core), GreenDays'14, WPMC'11, ISSC'10 (keynote), National Workshop of the CNRS GdR SoC-SiP 2009.

Tutorials

- 22nd IEEE/ACM Design, Automation and Test in Europe (DATE), March 2019 on "A Comprehensive Analysis of Approximate Computing Techniques: From Component to Application Level" [BMS19].
- Embedded Systems Week (ESWEEK), September 2018 on "A Comprehensive Analysis of Approximate Computing Techniques: From Component to Application Level" [BMS18].
- Hipeac Conference, January 2016 on "Fixed-point refinement, a guaranteed approach towards energy efficient computing" [SMPN16].
- Other Tutorials: DATE'15 [SMNP15], DATE'14 [SMNP14], WUPS'11.
- Tool Demonstrations: DATE'19, DAC'13, DAC'12, DATE'15, DATE'14, DATE'13, DATE'09, DATE'11, WPMC'11, ITEA Symposium 2009.
- Seminars: Calypto Design Systems (San Jose), Univ. of Massachusetts at Amherst (USA), Laval Univ. (CA), and 5 in France.

Summer Schools

- Member of the steering committee of a CNRS spring school for graduate students on embedded systems architectures and associated design tools (ARCHI) *(école sur les architectures des systèmes matériels enfouis et méthodes de conception associées).*

- Member of the steering committee of FETCH winter school on heterogeneous system design *(école d'hiver francophone sur les technologies de conception des Systèmes embarqués hétérogènes).*
- Co-organization of FETCH in Saint Malo, France, January 2018.
- Invited talk at FETCH, Saint Malo, France, January 2018 on "Playing with number representations for energy efficiency: an introduction to approximate and stochastic computing".
- Invited talk at FETCH, Mont Tremblant, Canada, January 2017 on "Need more Energy Efficiency? Agree to Compute Inexactly".
- Invited course at ARCHI Spring School, Nancy, France, March 2017 on "Design of VLSI Integrated Circuits – A (very) deep dive into processors".
- Invited talk at FETCH, Villard-de-Lans, France, in January 2016 on "Approximate Computing and Flexible Circuits for the IoT".
- Member of the steering committee of the French CNRS spring school for graduate students on low power real-time embedded systems (ECOFAC), *(école thématique sur la conception faible consommation pour les systèmes embarqués temps réel).*
- Co-organized ARCHI'2009 spring school in Pleumeur-Bodou, March 30–April 3, 2009.
- Co-organized ECOFAC'2010 spring school in Plestin les Grèves, March 29–April 2, 2010.
- Other Presentations in Summer Schools: FETCH (2015, 2014, 2012), ECOFAC (2012, 2010, 2006), ARCHI (2009, 2007, 2005).

8 PhD Supervisions

- Supervision or co-supervision of **49 defended PhD Theses**. One is Senior Research Director at CNRS, one Professor (INSA Rennes), eight Associate Professors (ENSSAT, INSA Rennes, ENSICaen, IUT de Lannion, Vietnam, Tunisie, Estonia), four researchers at CEA, and the others are engineers in industry or Postdocs.
- Supervision or co-supervision of 6 on-going PhD theses.
- Recipient of **PEDR** since 1998 (renewing in 2002, 2006, 2010, 2014, 2018).

On-going PhDs

1. Guillaume Lomet, Guess What I'm Learning: Side-Channel Analysis of Edge AI Training Accelerators, Oct. 2022, co-supervised with C. Killian.
2. Benoit Coqueret, attaques physiques contre des algorithmes à base d'intelligence artificielle, Oct. 2022, co-supervised with M. Carbone and G. Zaid (CESTI Thales Toulouse).
3. Sami Ben Ali, Efficient Low-Precision Training for Deep Learning Accelerators, Jan. 2022.
4. Amélie Marotta, Emp-error: EMFI-Resilient RISC-V Processor, Oct. 2021, co-supervised with R. Lashermes (Inria).
5. Léo De La Fuente, In-Memory Computing for Ultra-Low-Power Architectures, Nov. 2021, co-supervised with J.-F. Christmann (CEA List).
6. Cédric Gernigon, Highly compressed/quantized neural networks for FPGA on-board processing in Earth observation by satellite, Oct. 2020, co-supervised with S. Filip.

Defended PhDs

1. Thibault Allenet, Quantization and Adversarial Robustness of Embedded Deep Neural Networks, March 2023, co-supervised with O. Bichler (CEA List). Committee: K. Bailly (R), F. Yang (R), A. Bosio, P-A. Moellic. Currently Research Engineer at CEA, Saclay.
2. Van Phu Ha, Contributions to the Scalability of Automatic Precision Tuning, March 2023. Committee: F. de Dinechin (R), G. Caffarena (R), F. Jézéquel, D. Ménard. Currently Research Engineer at Secure-IC, Rennes.
3. Davide Pala, Microarchitectures for Robust and Efficient Incremental Backup in Intermittently Powered Systems, Nov. 2018, co-supervised with I. Miro-Panades (CEA Leti). Committee: A. Gamatié (R), T. Risset (R), D. Etiemble, M. Méndez Real. Currently Research Engineer at Cadence, Ireland.

4. Joel Ortiz Sosa, Design of a Digital Baseband Transceiver for Wireless Network-on- Chip Architectures, Dec. 2020, co-supervised with C. Roland (Lab-STICC). Committee: D. Morche (R), O. Romain (R), J.-P. Diguet, F. Petrot, N. Deltimple. Currently Senior R&D Engineer at Tekalis, Lannion.
5. Mael Gueguen, Frequent Itemset Sampling of High Throughput Streams on FPGA Accelerators, Oct. 2020, co-supervised with A. Termier (INRIA Lacodam). Committee: F. Petrot (R), M. Plantevit (R), L. Pierre, B. Negrevergne. Currently FPGA Design Engineer at Elsys Design, Lannion.
6. Rafail Psiakis, Performance Optimization Mechanisms for Fault-Resilient VLIW Processors, Dec. 2018, co-supervised with A. Kritikakou. Committee: A. Virazel (R), A. Bosio (R), S. Pillement, G. Keramidas. Currently Sr. Embedded Security Researcher at Technology Innovation Institute, Abu Dhabi Emirate.
7. Van-Dung Pham, Architectural Exploration of Network Interface for Energy Efficient 3D Optical Network-on-Chip, Dec. 2018, co-supervised with C. Killian and D. Chillet. Committee: V. Fresse (R), C. Tanougast (R), S. Niar, S. Le Beux. Now Research Eng. at Xlim Laboratory, Limoges.
8. Benjamin Barrois, Methods to Evaluate Accuracy-Energy Trade-Off in Operator-Level Approximate Computing, Dec. 2017. Committee: M. Duranton (R), A. Bosio (R), D. Menard, A. Tisserand, A. Molnos. Currently CTO and Co-Funder at Hiventive, Bordeaux.
9. Baptiste Roux, Methodology and Tools for Energy-aware Task Mapping on Heterogeneous Multiprocessor Architectures, Nov. 2017, co-supervised with M. Gautier. Committee: V. Fresse (R), F. Rousseau (R), B. Granado, L. Lagadec, J.-P. Delahaye. Currently Digital Design Engineer at IC'ALPS, Grenoble.
10. Rengarajan Ragavan, Error Handling and Energy Estimation Framework For Error Resilient Near-Threshold Computing, Sep. 2017, co-supervised with C. Killian. Committee: E. Beigné (R), P. Girard (R), L. Anghel (P), D. Menard. Currently Senior Lead Engineer at Qualcomm, Bengaluru, India.
11. Xuan-Chien Le, Improving Performance of Non-Intrusive Load Monitoring with Low-Cost Sensor Networks, Apr. 2017, co-supervised with B. Vrigneau. Committee: J.-F. Diouris (R), L. Clavier (R), S. Bacha (P), D. Menga, B. Leprettre, C. Langlais.
12. Florent Berthier, Design of an Ultra Low Power Processor for Wireless Sensor Networks, Dec. 2016, co-supervised with E. Beigné (CEA Leti). Committee: L. Lacassagne (R), P. Benoit (R), Ian O'Connor (P), J.-L. Nagel. Now Engineer at Semtech, Grenoble.
13. Christophe Huriaux, Enhanced FPGA Architecture and CAD Flow for Efficient Runtime Hardware Reconfiguration, Dec. 2015, co-supervised with A. Courtay. Committee: G. Lemieux (R), L. Torres (R), L. Anghel, P. Millet, R. Tessier. Currently Hardware and Embedded Systems R&D Engineer at Digidia, Rennes.
14. Pramod Udupa, Low Complexity, Parallel Algorithms and Scalable Architectures for Real Time Coherent Optical OFDM Systems, June 2014, co-supervised with L. Bramerie (Foton). Committee: E. Boutillon (R), C. Jego (R), L. Bossuet, E. Pincemin, M. Jezequel. Now Engineer at Signalchip Innovations Pvt. Ltd, Bangalore.
15. Ganda-Stéphane Ouedraogo, Automatic Synthesis of Hardware Accelerators from High-Level Specifications of Physical Layer Waveform for Flexible Radio, Dec. 2014, co-supervised with M. Gautier. Committee: T. Risset (R), R. Pacalet (R), C. Moy, D. Noguet. Now Research Engineer at NestWave, Paris.
16. Matthieu Texier, Dynamic Parallelism Management in Multi-Core Architectures for Mobile Systems, Dec. 2014, co-supervised with R. David and K. Benchehida (CEA). Committee: F. Rousseau (R), A. Pegatoquet (R), J.P. Diguet, H.-P. Charles. Now Engineer Krono-Safe, Saclay, France.
17. Trong Nhan Le, Global Power Manager System for Self-Powered Autonomous Wireless Sensor Node, June 2014, co-supervised with O. Berder and A. Pégatoquet (U. Nice). Committee: J.F. Diouris (R), C.D. Pham (R), M. Magno, C. Bernier, J.P. Diguet. Now PostDoc U. Nice.
18. Amine Didioui, Energy-Aware Transceiver for Energy Harvesting Wireless Sensor Networks, Oct. 2014, co-supervised with C. Bernier (CEA LETI). Committee: D. Dallet (R), F. Mieyeville (R), S. Bourdel, R. Briand, R.M. Sauvage. Now Research Engineer at SEB R&D, Lyon, France.
19. Robin Bonamy, Power Consumption Modeling and Optimisation for Reconfigurable Platform, July 2013, co-supervised with D. Chillet and S. Bilavarn (LEAT, Nice). Committee: M. Renovell (R), C. Piguet (R), E. Senn, C. Jego. Now Research Engineer, CNRS, Nice.

20. Mahtab Alam, Power Aware Adaptive Techniques for Wireless Sensor Networks, 26 Feb. 2013, co-supervised with D. Menard and O. Berder. Committee: E. Popovici (R), T. Risset (R), A. Pegatoquet. Now Research Scientist, Qatar Mobility Innovations Center. Now Research Scientist, Qatar Mobility Innovations Center.
21. Vivek Tovinakere Dwarakanath, Ultra-Low Power Reconfigurable Architectures for Controllers in Wireless Sensor Network Nodes, 12 Feb. 2013, co-supervised with S. Derrien. Committee: P. Girard (R), M. Belleville (R), J.P. Diguet, I. O'Connor. Now a Senior Architect in Nvidia, Bangalore.
22. Vinh Tran, Energy Optimisation of Cooperative Transmissions for Wireless Sensor Networks, Dec. 2012, co-supervised with O. Berder. Committee: J.M. Gorce (R), J.F. Diouris (R), L. Deneire, P. Mary. Now PostDoc, CEA Leti, Grenoble, France.
23. Karthick Parashar, System-level Approach for Implementation and Optimization of Signal Processing Applications into Fixed-Point Architectures, Dec. 2012, co-supervised with D. Menard. Committee: C. Carreras (R), C. Jego (R), F. Catthoor, A. Jerraya. Now Researcher, IMEC, Leuven, Belgique, formerly PostDoc, Imperial College, London, UK.
24. Antoine Eiche, Real-Time Scheduling for Heterogeneous and Reconfigurable Architectures using Neural Network Structures, Sep. 2012, co-supervised with D. Chillet and S. Pillement. Committee: O. Temam (R), Y. Trinquet (R), E. Martin, D. Demigny. Now Engineer, Mandriva, Paris, France.
25. Hai Nam Nguyen, Numerical Accuracy Optimization for Low-Power Embedded Systems, Dec. 2011, co-supervised with D. Menard. Committee: M. Jezequel (R), L. Fesquet (R), C. Moy, F. Horlin, D. Noguet. Now Engineer, Open Web Solutions, Paris, France.
26. Adeel Pasha, System-Level Synthesis of Ultra Low-Power Wireless Sensor Network Node Controllers: A Complete Design-Flow, Dec. 2010, co-supervised with S. Derrien. Committee: C. Piguet (R), F. Petrot (R), C. Belleudy, T. Risset. Now Assistant Professor at LUMS (Lahore Univ. of Management Sciences), School of Science and Engineering, Lahore, Pakistan.
27. Erwan Grace, Memory-Oriented Reconfigurable Embedded Architecture, oct. 2010, co-supervised with D. Chillet and R. David (CEA). Now with Alcatel-Lucent.
28. Tuan Duc Nguyen, Cooperative MIMO Strategies for Energy Constrained Wireless Sensor Networks, may 2009, co-supervised with O. Berder. Committee: JM. Gorce (R), JF. Diouris (R) E. Boutillon (P), M. Dohler. Now Assistant Professor at International University - Vietnam National Univ. - Hochiminh City.
29. Renaud Santoro, High-Rate True Random Number Generators with Guaranteed Quality, dec. 2009, co-supervised with S. Roy (Laval Univ., CA), cotutelle. Now with Alcatel-Lucent. Committee: B. Rouzeyre (R), R. Tessier (R) V. Fischer (P), P. Fortier.
30. Antoine Courtay, Power Consumption of On-Chip Interconnections: High-Level Estimation and Architecture-Level Optimizations, nov. 2008, co-supervised with J. Laurent (LESTER, Lorient). Now Assistant Professor at Univ. Rennes 1 (ENSSAT), formerly a PostDoc at Univ. Nice. Committee: M. Belleville (R), B. Rouzeyre (R) S. Piestrak (P), Y. Leduc.
31. Julien Lallet, Mozaïc: a Generic Platform for Modeling and Design of Dynamically Reconfigurable Architectures, nov. 2008, co-supervised with S. Pillement. Now with Alcatel-Lucent after a PostDoc at the Heinz Nixdorf Institut of Univ. Paderborn. Committee: L. Torres (R), B. Granado (R) S. Piestrak (P), L. Lagadec.
32. Mickael Cartron, Energy Optimization of Wireless Sensor Networks, dec. 2006. Now Researcher at CEA List Saclay. Committee: M. Auguin (R), J.F. Diouris (R), P. Garda.
33. Romuald Rocher, Accuracy and Range Evaluation of Fixed-Point Systems, dec. 2006, co-supervised with D. Menard. Now Assistant Professor at Univ. Rennes 1 (IUT de Lannion). Committee: J.M. Brossier (R), M. Bellanger(R), G. Demoment.
34. Faten Ben Abdallah, Étude et optimisation de l'interaction processeurs-architectures reconfigurables dynamiquement, 2009. Thèse en cotutelle avec l'ENI de Tunis. Actuellement maître assistant à l'ENISo (Tunisie). Jury: M. Paindavoine (R), R. Bouallegue (R), G. Gogniat.
35. Taofik Saïdi, Architectures pour les communications MIMO avec échantillonnage parallèle et adaptatif, 2008. Thèse en cotutelle avec l'Université Laval, Québec, Canada. Actuellement ingénieur chez Amesys. Jury: JL. Danger (R), JF. Frigon (R), P. Fortier.
36. Imène Benkermi, Système d'exploitation temps réel pour architectures parallèles reconfigurables hétérogènes,

2007. Ingénieur chez Valeo. Jury: B. Granado (R), J.P. Diguet (R), Y. Trinquet.

37. Nicolas Hervé, Méthodologie de conception des architectures reconfigurables en précision finie, 2007. Actuellement en Post-Doc à l'Université de Sao Paulo au Brésil. Jury: B. Rouzeyre (R), T. Risset (R), J.L. Philippe.
38. Ekué Kinvi-Boh, Architectures de systèmes intégrés en logique ternaire, soutenue en novembre 2006. Actuellement ingénieur dans une société de service. Jury: D. Etiemble (R), S. Piestrak (R), J.D Legat.
39. Stéphane Chevobbe, Unité de commande pour systèmes parallèles : contrôleur basé sur l'implémentation dynamique de réseaux de Pétri, 2005. Actuellement chercheur au CEA Saclay. Jury: M. Auguin (R), A. Mérigot (R), J.D Legat, D. Demigny.
40. Jean-Marc Philippe, Intégration des réseaux sur silicium : optimisation des performances des couches physique et liaison, 2005. Actuellement chercheur au CEA Saclay. Jury: G. Cambon (R), S. Roy (R), J.P. Diguet, C. Gamrat.
41. Raphaël David, Architecture reconfigurable dynamiquement pour applications mobiles, 2003. Actuellement chercheur au CEA Saclay. Jury: G. Cambon (R), D. Demigny (R), T. Collette, D. Lavenier.
42. Raofeng Yu, Estimation de haut niveau du placement et des interconnexions de circuits VLSI submicroniques, 2002. Actuellement ingénieur dans une société chinoise. Jury: A. Mérigot (R), S. Piestrak (R), E. Martin.
43. Alexandre Buisson, Implémentation efficace d'un codeur vidéo hiérarchique granulaire sur une architecture multi-pentium, 2002. Ingénieur chez Nextamp, Rennes. Jury: JM. Chassery (R), R. Prost (R), S. Pateux, P. Sainrat.
44. Daniel Ménard, Méthodologie de compilation d'algorithmes de traitement du signal en précision infinie pour les processeurs en virgule fixe, 2002. Actuellement MCF à l'ENSSAT, Lannion Jury: D. Demigny (R), T. Risset (R), E. Martin, P. Le Guernic.
45. Matthieu Denoual, Estimation au niveau architectural de la consommation des systèmes intégrés dédiés au traitement numérique du signal, 2001. Post-doc au LIMMS à Tokyo (Japon). Actuellement MCF à l'ENSICaen. Jury: B. Rouzeyre (R), C. Piguet (R), E. Martin, D. Lavenier.
46. Joseph Dedou, Synthèse architecturale des systèmes asynchrones, 2000. Ingénieur à Mitsubishi R&D Jury: A. Mérigot (R), S. Piestrak (R), E. Martin, J.D. Legat.
47. Jean-Gabriel Cousin, Méthodologie de conception de coeurs de processeurs spécifiques : mise en oeuvre sous contraintes, estimation de la consommation, 1999. Actuellement MCF à l'INSA de Rennes. Jury: M. Auguin (R), J.L. Philippe (R), J.P. Calvez, S. Rajopadhye.
48. Daniel Chillet, Méthodologie de conception architecturale des mémoires pour circuits dédiés au traitement du signal temps réel, 1997. Actuellement MCF à l'ENSSAT, Lannion. Jury: F. Catthoor (R), J.P. Calvez (R), E. Martin, J.L. Philippe.
49. Jean-Philippe Diguet, Estimation de complexité et transformations d'algorithmes de traitement du signal pour la conception de circuits VLSI, 1996. Actuellement CR1 CNRS au LESTER, Lorient. Jury: Y. Sorel (R), P. Duhamel (R), M. Arndt.

9 Research Collaborations and Funding

9.1 Collaborations

International collaborations with: University of British Columbia, Vancouver, Canada; University College Cork, Ireland; EPFL, Switzerland; IMEC, Belgique; Québec University at Trois-Rivières, Canada; Laval University, Québec, Canada; University of Massachusetts, Amherst, USA; IIT Goa, India; Tallinn University of Technology, Estonia; Politecnico di Milano, Italy; Universidad Politécnica de Madrid, Spain; Concordia University, Canada; Southeast University, Nanjing, China.

Inria *associated teams* and other international projects:

- DeLeES, Energy-efficient Deep Learning Systems for Low-cost Embedded Systems, University of British Columbia, Vancouver, Canada, Prof. Guy Lemieux, France-Canada Research Fund (FCRF).
- IntelliVIS: Design Automation for Intelligent Vision Hardware in Cyber Physical Systems, Inria As-

sociated Team (2019-2021) with IIT Goa, India, Prof. Sharad Sinha on the design and development of artificial intelligence based embedded vision architectures for cyber physical systems.
- IOTA, Ultra-Low Power Computing Platform for IoT leveraging Controlled Approximations, INRIA Associated Team (2017-2019) with Ecole Polytechnique Fédérale de Lausanne, Switzerland, Prof. Christian Enz on ultra low power hardware design, approximate operators and functions, accuracy analysis, and static and dynamic energy management.
- HARDIESSE, Heterogeneous Accelerators for Reconfigurable DynamIc, Energy efficient, Secure SystEms, INRIA Associated Team (2014-2016) with University of Massachusetts at Ahmerst, US, Prof. Russel Tessier and Prof. Maciej Ciesielski, on the study new reconfigurable structures for hardware accelerators with specific focus on: energy efficiency, runtime dynamic reconfiguration, protections against physical attacks, and verification.
- SPiNaCH, Secure and low-Power sensor Networks Circuits for Healthcare embedded applications, CNRS PICS int. project (2012 - 2014) with Code&Crypto group, University College Cork, Ireland, Prof. Liam Marnane and Prof. Emanuel Popovici on arithmetic operators for cryptography, side channel attacks for security evaluation, energy-harvesting sensor networks, and sensor networks for health monitoring.
- ASTER - Architectures for Efficient Reconfigurable Mobile Telecommunication Systems, Inria International Program, Associate Team with Université Laval (S. Roy), Canada (2007-2009).

Recent publications with foreign colleagues: [ABHB+16, CAL+17, **?**, **?**, MCL+19a, MCL+19b, HST16, LKLB+18, CSM+11b, ABHB+16, SOB+13, CSM+12, NMCS12, HST16, BPS16, JSK+15, SMNP15, HST14b, SMNP14, LMP+13, GAV+12, BHS+12, TRS10, PRM+10, SSR09a, SSR09b, STSR09, HST14a, SOB+12, MNR+10]

Collaborations with other Labs in France: DGA, CEA Leti, INL, FOTON Institute, LRMM, IETR, LEAT, Lab-STICC, and Inria Pacap, Socrate and Lacodam.

Recent publications with colleagues from other Labs in France: [LKLB+18, RGSD20, NSG+18, NGGA+17, NSG+17, MCL+19a, MCL+19b, BBH+17, BMS19, BMS18, BBH+16a, MDSM19, BBCS16, SSR18, SSRK19, SSR19, NSG+16a, NSG+16b, SSLB+16, LEP+17, LKLB+18, LKLB+18, LPK+18, SMPN16, CAL+17, BCC+18, GST19]

9.2 Funding of Research Projects and Platforms

On-Going Grants
- **ANR Re-Trusting**, *REliable hardware for TRUSTworthy artificial INtelliGence*. Collaboration with INL, LIP6,THALES. 2021-2025. 205k€.
- **LeanAI**, *Dynamic Precision Training on the Edge*, funded by labex CominLabs. Collaboration with LS2N, LIP. 2021-2024. 150k€.
- **ANR AdequateDL**, *Approximating Deep Learning Accelerators*. Collaboration with LIRMM, INL, CEA LIST. 2019-2022. 210k€. I am the coordinator of this project.
- **ANR Rakes**, *Radio Killed an Electronic Star – Wireless Network on Chip for shared memory many-core architectures*. Collaboration with TIMA, Lab-STICC. 2019-2023. 205k€.
- **ANR Opticall2**, *on-chip OPTIcal interconnect for ALL to ALL communications*. Collaboration with INL, C2N, CEA-LETI, Kalray. 2018-2023. 195k€.
- **Intel Hardware Accelerator Research Program**, *Heterogeneous Multi-Core Architectures and (Approximate) Compilers*. Access to Intel Xeon+FPGA system (Broadwell + Arria10) platforms and tools via remote access to a centralized cluster installation. 2017-.
- **CPER SmartSense:**, An Open Platform for Smart Building Research, 2015-2022. 400k€.
- **Sniffer**, *Non-Intrusive Surveillance of Mains Operated Equipment*, DGA call on AI. 2020-2023. 312k€.

Recent Past Grants
- **RAPID Flodam**, *Software Flow to Harden Multicore Architectures*. Collaboration with Temento, Onera. 2017-2021. 280k€.
- **Inria Project Lab ZEP**, *ZEro Power computing systems*. Collaboration with Inria Socrate, Pacap, Corse, CEA LETI. 2017-2020. ≈ 200k€.

- **ANR Project ARTEFaCT**, *AppRoximaTivE Flexible Circuits and Computing for IoT*. Collaboration with EPFL, CSEM, CEA LETI. 2016-2019. 214k€.
- **H2020 ARGO**, *WCET-Aware Parallelization of Model-Based Applications for Heterogeneous Parallel Systems*. Collaboration with KIT (GE), SCILAB enterprises (FR), UR1 (FR), EMMTRIX (GE), TEI (GR), Absint (GE), Fraunhofer (GE). 2016-2018. 554 k€.
- **BBC**, *Wireless Interconnect Network on chip for Broadcast-Based parallel Computing*, funded by labex CominLabs. INRIA, Lab-STICC (Lorient, Brest). 2016-2019. 140k€.
- **3DCORE**, *3D Many-Core Architectures based on Optical Network on Chip*, funded by labex CominLabs. INRIA, FOTON, INL (Lyon). 2014-2017. 290k€.
- **BoWI-BPM**, *Body-World Interaction (follow-up)*, funded by labex CominLabs. INRIA, Lab-STICC (Lorient). 2017-2018. 80k€.
- **BoWI**, *Body-World Interaction: Towards an accurate gesture and body movement estimation using very-small and low-power wearable sensor nodes*, funded by labex CominLabs. IRISA, IETR, Lab-STICC (Lorient, Brest). 2012-2016. 402k€.
- **EMBRACE Project**, funded by Images and Networks competitiveness cluster for project with SMEs, EMBedded Radio ACcElerator. Collaboration with Digidia, PrimeGPS, 2014-2016. 172k€.
- **European Project *Future and Emerging Technologies (FET) Flagship Initiatives* "Guardian Angels for a Smarter Life"**, Zero-Power Systems: these small devices, products of nanotechnology, will combine low-power electronics with new sources of energy, taken form their immediate environment. Collaboration with about fifty academic and industrial partners such as EPFL, ETHZ, IMEC, KUL, UCL, CNRS, CEA LETI, VTT, TUM, Fraunhofer. http://www.ga-project.eu
- **European Project FP7 FLEXTILES**, Self Adaptive Heterogeneous Manycore Based on Flexible Tiles. Collaboration with Thales (FR), UR1 (FR), KIT (GE), TU/e (NL), CSEM (SW), CEA LETI (FR), Sundance (UK). 2011-2014. 380k€.
- **European Project FP7 ALMA**, Architecture oriented paraLlelization for high performance embedded Multicore systems using scilAb. Collaboration with KIT (GE), UR1 (FR), Recore Systems (NL), Univ. of Peloponnese (GR), TEI-MES (GR), Intracom SA (GR), Fraunhofer (GE). 2011-2014. 400k€.
- **Coordination of the French ANR Project DEFIS**, Design of Fixed-Point Systems. Collaboration with INRIA/CAIRN, LIP6, LIRMM, CEA LIST, Thales, Inpixal. 2011-2015. 252k€.

10 Collaborations with Industry and Technology Transfer

Collaborations with large companies: Kalray, Huawei, Safran, Thales, Nokia Bell Labs, Intel (HARP), STMicroelectronics, Thomson/Technicolor, Alcatel-Lucent, Orange Labs, Atmel, Phillips, Infineon.

Collaborations with SMEs: Temento Systems, Secure-IC, Digidia, PrimeGPS, Feichter Electronics, 3D Ouest, Athemium, Envivio, Geensys, Aphycare Technologies, SmartQuantum, Sensaris, Ditocom, Eca-Faros.

Recent publications with colleagues from industry: [PKS19, SOB+13, JSK+15, BDBS13, GAV+12, LMMA+12, BHS+12, SOB+12].

Recent Industrial Contracts:

Huawei Technologies (HiSilicon) in Sophia Antipolis is supporting the research on floating-point to fixed-point conversion. The company is interested in exploring accuracy/performance trade-off for its mobile phone Image Signal Processors (ISPs) chip using the TypEx tool. Grant: 130k€.

Safran will fund a PhD in 2020 to study the FPGA implementation of deep convolutional neural network under SWAP (Size, Weight And Power) constraints for detection, classification, image quality improvement of observation systems, and awareness functions (trajectory guarantee, geolocation by cross view alignment) applied to autonomous vehicle. This thesis will in particular consider pruning and reduced precision. Grant: PhD + 45k€.

Other direct funding was obtained from STMicroelectronics, Orange Labs and Thales through CIFRE grants or direct funding.

Technology Transfer and Startup: I was involved in the creation process of a startup around my expertise on automatic fixed-point conversion and error analysis. The company WeDoLow (formerly Yubik) was cre-

ated in 2022 after an incubation in the Startup Studio of Inria. I am now part of its Advisory Board.

The ID.Fix framework has been successfully tested and used by STMicroelectronics, Grenoble, for the design of a wireless digital transceiver. Its successor, TypEx, was successfully used by the Silicon division of Huawei Technologies (HiSilicon) in Sophia Antipolis, to help the company explore accuracy/performance trade-off for its mobile phone Image Signal Processors (ISPs) chipset.

Most of my former PhD students or PostDocs are now R&D engineers in companies or startups such as Synopsys, Qualcom, Thales, Intel, Nvidia, STMicroelectronics, Nokia, Altran, Huawei, Semtech, Secure-IC, IC'Alps, Hiventive, Kereval, Digidia.

Recent Publications (2018–2022)

International Journals

[FdSKERC+22] Fernando Fernandes dos Santos, Angeliki Kritikakou, Josie Esteban Rodriguez Condia, Juan David Guerrero Balaguera, Matteo Sonza Reorda, Olivier Sentieys, and Paolo Rech. Characterizing a neutron-induced fault model for deep neural networks. *IEEE Transactions on Nuclear Science*, 2022.

[LMKS22] Xinmei Li, Lei Mo, Angeliki Kritikakou, and Olivier Sentieys. Approximation-aware task deployment on heterogeneous multi-core platforms with dvfs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pages 1–15, 2022.

[PKS22] Rafail Psiakis, Angeliki Kritikakou, and Olivier Sentieys. Dynamic fault-tolerant vliw processor with heterogeneous function units. *Microprocessors and Microsystems: Embedded Hardware Design*, 93:104564, 2022.

[PMPS21] Davide Pala, Ivan Miro-Panades, and Olivier Sentieys. Freezer: A specialized nvm backup controller for intermittently-powered systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(8):1559–1572, 2021.

[KPCS20] Angeliki Kritikakou, Rafail Psiakis, Francky Catthoor, and Olivier Sentieys. Binary classification tree of rigid error detection and correction techniques. *ACM Computing Surveys*, 53(4):1–38, 2020.

[MKSC20] Lei Mo, Angeliki Kritikakou, Olivier Sentieys, and Xianghui Cao. Real-time imprecise computation tasks mapping for dvfs-enabled networked systems. *IEEE Internet of Things Journal*, 8(10):8246–8258, 2020.

[RGSD20] Baptiste Roux, Matthieu Gautier, Olivier Sentieys, and Jean-Philippe Delahaye. Energy-driven design space exploration of tiling-based accelerators for heterogeneous multiprocessor architectures. *Microprocessors and Microsystems*, 77:1–12, 2020.

[LKLB+18] Jiating Luo, Cédric Killian, Sebastien Le Beux, Daniel Chillet, Olivier Sentieys, and Ian O'Connor. Offline Optimization of Wavelength Allocation and Laser Power in Nanophotonic Interconnects. *ACM Journal on Emerging Technologies in Computing Systems*, 14(2):1 – 19, July 2018.

[MKS18a] Lei Mo, Angeliki Kritikakou, and Olivier Sentieys. Controllable QoS for Imprecise Computation Tasks on DVFS Multicores with Time and Energy Constraints. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, pages 1 – 14, July 2018.

[MKS18b] Lei Mo, Angeliki Kritikakou, and Olivier Sentieys. Energy-Quality-Time Optimized Task Mapping on DVFS-enabled Multicores. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pages 1 – 10, July 2018.

[NSG+18] Trung Hien Nguyen, Pascal Scalart, Mathilde Gay, Laurent Bramerie, Christophe Peucheret, Fausto Gomez Agis, Olivier Sentieys, Jean-Claude Simon, and Michel Joindot. New metric for IQ imbalance compensation in optical QPSK coherent systems. *Photonic Network Communications*, 36(3):326–337, December 2018.

Book

[BMS22] Alberto Bosio, Daniel Menard, and Olivier Sentieys. *Approximate Computing Techniques: From Component- to Application-Level*. Springer, 2022.

Book Chapters

[DFS+22] Etienne Dupuis, Silviu-Ioan Filip, Olivier Sentieys, David Novo, Ian O'Connor, and Alberto Bosio. *Approximate Computing Techniques - From Component- to Application-Level*, chapter Approximations in Deep Learning. Springer, 2022.

[SM22] Olivier Sentieys and Daniel Menard. *Approximate Computing Techniques - From Component- to Application-Level*, chapter Customizing Number Representation and Precision. Springer, 2022.

[MCL+19a] Daniel Menard, Gabriel Caffarena, Juan Antonio Lopez, David Novo, and Olivier Sentieys. Fixed-point refinement of digital signal processing systems. In *Digitally Enhanced Mixed Signal Systems*, pages 1–37. The Institution of Engineering and Technology, May 2019.

[MCL+19b] Daniel Ménard, Gabriel Caffarena, Juan Antonio Lopez, David Novo, and Olivier Sentieys. Analysis of Finite Word-Length Effects in Fixed-Point Systems. In *Handbook of Signal Processing Systems*, pages 1063–1101. Springer, 2019.

[MKS18d] Lei Mo, Angeliki Kritikakou, and Olivier Sentieys. Imprecise Computation Task Mapping on Multi-Core Wireless Sensor Networks. In *Encyclopedia of Wireless Networks*, pages 1 – 6. October 2018.

Keynotes, Invited Conferences, and Tutorials

[Sen22] Olivier Sentieys. Opportunities for computer architecture research with open-source hardware - The case of RISC-V. In *Journées Scientifiques Inria (JSI)*, November 2022.

[Sen21a] Olivier Sentieys. Approximate deep learning accelerators: Improving performance and energy efficiency of deep-learning hardware accelerators with controlled arithmetic approximations. In *CSW 2021 - HiPEAC Computing Systems Week*, October 2021.

[Sen21b] Olivier Sentieys. An optimization playground for precision and number representation tuning. In *Report from Dagstuhl Seminar 21302 - Approximate Systems*, July 2021.

[Sen19] Olivier Sentieys. Playing with Numbers for Energy Efficiency: an Introduction to Approximate Computing. In *Keynote at the IEEE International Nanodevices and Computing (INC) - IEEE International Conference on Rebooting Computing (ICRC)*, Grenoble, France, April 2019. IEEE.

[BMS19] Alberto Bosio, Daniel Menard, and Olivier Sentieys. A Comprehensive Analysis of Approximate Computing Techniques: From Component- to Application-Level. Tutorial at 22nd IEEE/ACM Design, Automation and Test in Europe (DATE), March 2019.

[BMS18] Alberto Bosio, Daniel Menard, and Olivier Sentieys. A Comprehensive Analysis of Approximate Computing Techniques: From Component- to Application-Level. Tutorial at Embedded Systems Week (ESWEEK), September 2018.

[Sen18] Olivier Sentieys. Playing with Number Representations and Operator-Level Approximations. In *Keynote at the Third Workshop on Approximate Computing (AxC), in conjunction with IEEE European Test Symposium (ETS)*, June 2018.

Main International Conferences

[HS23] Van-Phu Ha and Olivier Sentieys. Maximizing computing accuracy on resource-constrained architectures. In *26th IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1–6, 2023.

[TKS23] Marcello Traiola, Angeliki Kritikakou, and Olivier Sentieys. hardnning: a machine-learning-based framework for fault tolerance assessment and protection of deep neural networks. In *26th IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1–6, 2023.

[KSH+22] Angeliki Kritikakou, Olivier Sentieys, Guillaume Hubert, Youri Helen, Jean-Francois Coulon, and Patrice Deroux-Dauphin. Flodam: Cross-layer reliability analysis flow for complex hardware designs. In *25th IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1–6, March 2022.

[ABBS22] Thibault Allenet, David Briand, Olivier Bichler, and Olivier Sentieys. Disentangled loss for low-bit quantization-aware training. In *IEEE/CVF Computer Vision and Pattern Recognition Conference (CVPR)*, Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR) Workshops, pages 2788–2792, 2022.

[dSRKS22] Fernando Fernandes dos Santos, Paolo Rech, Angeliki Kritikakou, and Olivier Sentieys. Evaluating the impact of mixed-precision on fault propagation for deep neural networks on GPUs. In *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 327–327, 2022.

[FdSKS22] Fernando Fernandes dos Santos, Angeliki Kritikakou, and Olivier Sentieys. Experimental evaluation of neutron-induced errors on a multicore risc-v platform. In *28th IEEE International Symposium on OnLine Testing and Robust System Design (IOLTS)*, pages 1–7, 2022.

[FdSKSR22] Fernando Fernandes dos Santos, Angeliki Kritikakou, Olivier Sentieys, and Paolo Rech. Characterizing deep neural networks neutrons-induced error model. In *IEEE Nuclear & Space Radiation Effects Conference (NSREC)*, pages 1–5, 2022.

[KNRF+22] Angeliki Kritikakou, Panagiota Nikolaou, Ivan Rodriguez-Ferrandez, Joseph Paturel, Leonidas Kosmidis, Maria K. Michael, Olivier Sentieys, and David Steenari. Functional and timing implications of transient faults in critical systems. In *28th IEEE International Symposium on OnLine Testing and Robust System Design (IOLTS)*, pages 1–10, 2022.

[TFW+22] Mariko Tatsumi, Silviu-Ioan Filip, Caroline White, Olivier Sentieys, and Guy Lemieux. Mixing low-precision formats in multiply-accumulate units for dnn training. In *IEEE International Conference on Field Programmable Technology (FPT)*, pages 1–9, 2022.

[HS21] Van-Phu Ha and Olivier Sentieys. Leveraging bayesian optimization to speed up automatic precision tuning. In *24th IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1–6, February 2021.

[SFB+21] Olivier Sentieys, Silviu-Ioan Filip, David Briand, David Novo, Etienne Dupuis, Ian O'Connor, and Alberto Bosio. AdequateDL: Approximating deep learning accelerators. In *DDECS 2021 - 24th International Symposium on Design and Diagnostics of Electronic Circuits and Systems*, pages 37–40. IEEE, 2021.

[HYS20] Van-Phu Ha, Tomofumi Yuki, and Olivier Sentieys. Towards Generic and Scalable Word-Length Optimization. In *IEEE/ACM Design Automation and Test in Europe (DATE)*, pages 1–6, Grenoble, France, March 2020.

[PKS20] Joseph Paturel, Angeliki Kritikakou, and Olivier Sentieys. Fast cross-layer vulnerability analysis of complex hardware designs. In *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 328–333, Limassol, Cyprus, July 2020. IEEE.

[RPPS19b] Simon Rokicki, Davide Pala, Joseph Paturel, and Olivier Sentieys. What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications. In *38th IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 1–8, Westminster, CO, United States, November 2019. IEEE.

[GST19] Mael Gueguen, Olivier Sentieys, and Alexandre Termier. Accelerating Itemset Sampling using Satisfiability Constraints on FPGA. In *22nd IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1046–1051, Florence, Italy, March 2019. IEEE.

[MKS19] Lei Mo, Angeliki Kritikakou, and Olivier Sentieys. Approximation-aware Task Deployment on Asymmetric Multicore Processors. In *22nd IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1513–1518, Florence, Italy, March 2019. IEEE.

[PKS19] Rafail Psiakis, Angeliki Kritikakou, and Olivier Sentieys. Fine-Grained Hardware Mitigation for Multiple Long-Duration Transients on VLIW Function Units. In *22nd IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 976–979, Florence, Italy, March 2019. IEEE.

[SSRK19] Joel Ortiz Sosa, Olivier Sentieys, Christian Roland, and Cédric Killian. Multi-Carrier Spread-Spectrum Transceiver for WiNoC. In *13th IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, pages 1–2, New York, United States, October 2019. ACM.

[SSR19] Joel Ortiz Sosa, Olivier Sentieys, and Christian Roland. Adaptive Transceiver for Wireless NoC to Enhance Multicast/Unicast Communication Scenarios. In *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 1–6, Miami, United States, July 2019. IEEE.

[MDSM19] Oumaima Matoussi, Yves Durand, Olivier Sentieys, and Anca Molnos. Error Analysis of the Square Root Operation for the Purpose of Precision Tuning: a Case Study on K-means. In *30th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 1–8, New York, United States, July 2019. IEEE.

[SSR18] Joel Ortiz Sosa, Olivier Sentieys, and Christian Roland. A Diversity Scheme to Enhance the Reliability of Wireless NoC in Multipath Channel Environment. In *IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, Torino, Italy, October 2018.

[MKS18c] Lei Mo, Angeliki Kritikakou, and Olivier Sentieys. Energy-Quality-Time Optimized Task Mapping on DVFS-enabled Multicores. In *IEEE/ACM Embedded Systems Week (ESWEEK)*, pages 1–11, Torino, Italy, September 2018.

[CLGB+18] Antoine Courtay, Mickaël Le Gentil, Olivier Berder, Arnaud Carer, Pascal Scalart, and Olivier Sentieys. Zyggie: A Wireless Body Area Network platform for indoor positioning and motion tracking. In *IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5, Florence, Italy, May 2018. IEEE.

Other International Conferences and Workshops (lower selectivity, posters)

[FKS22] Fernando Fernandes, Angeliki Kritikakou, and Olivier Sentieys. Experimental evaluation of neutron-induced errors on a risc-v processor. In *Spring 2022 RISC-V Week*, 2022. Poster.

[RPS22] Simon Rokicki, Joseph Paturel, and Olivier Sentieys. Comet: a risc-v core synthesized from C++ specifications. In *Spring 2022 RISC-V Week*, 2022. Poster.

[TXW+21] Mariko Tatsumi, Yuxiang Xie, Caroline White, Silviu-Ioan Filip, Olivier Sentieys, and Guy Lemieux. Mptorch and mparchimedes: Open source frameworks to explore custom mixed- precision operations for dnn training on edge devices. In *ROAD4NN 2021 - 2nd ROAD4NN Workshop: Research Open Automatic Design for Neural Networks*, December 2021.

[RVS19] Nicolas Roux, Baptiste Vrigneau, and Olivier Sentieys. Improving NILM by Combining Sensor Data and Linear Programming. In *IEEE Sensors Applications Symposium (SAS)*, pages 1–6, Sophia Antipolis, France, March 2019. IEEE.

[PKSC19] Rafail Psiakis, Angeliki Kritikakou, Olivier Sentieys, and Emmanuel Casseau. Run-time Coarse-Grained Hardware Mitigation for Multiple Faults on VLIW Processors. In *Conference on Design and Architectures for Signal and Image Processing (DASIP)*, pages 1–6, Montréal, Canada, October 2019.

[RPPS19a] Simon Rokicki, Davide Pala, Joseph Paturel, and Olivier Sentieys. What You Simulate Is What You Synthesize: Design of a RISC-V Core from C++ Specifications. In *RISC-V Workshop*, pages 1–2, Zurich, Switzerland, June 2019.

[HYS19] Van-Phu Ha, Tomofumi Yuki, and Olivier Sentieys. Noise Budgeting in Multiple-Kernel Word-Length Optimization. In *4th Workshop on Approximate Computing (AxC)* , pages 1–3, Florence, Italy, March 2019.

[LPK+18] Jiating Luo, Van-Dung Pham, Cédric Killian, Daniel Chillet, Ian O'Connor, Olivier Sentieys, and Sébastien LE BEUX. Run-Time management of energy-performance trade-off in Optical Network-on-Chip. In *XXXIII Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–6, Lyon, France, November 2018.

[BCC+18] Gautier Berthou, Arnaud Carer, Henri-Pierre Charles, Steven Derrien, Kevin Marquet, Ivan Miro-Panades, Davide Pala, Isabelle Puaut, Fabrice Rastello, Tanguy Risset, Erven Rohou, Guillaume Salagnac, Olivier Sentieys, and Bharam Yarahmadi. The INRIA ZEP project: NVRAM and Harvesting for Zero PowerComputations. 10th Annual Non-Volatile Memories Workshop (NVMW), March 2018. Poster.

[RVS18] Nicolas Roux, Baptiste Vrigneau, and Olivier Sentieys. Estimating Power Loads from Partial Appliance States. 4th International Workshop on Non-Intrusive Load Monitoring (NILM), March 2018. Poster.

Main Publications (2008–2016)

Special Issues of Journals

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