High-Level Synthesis for Multicore Processor Design and Specialization

(is C-based design suitable to complex architectures such as a RISC-V multicore processor?)

Position: Research Engineer/Research Associate

Keywords: processor architecture, multicore, hardware accelerator, high-level synthesis, FPGA design, RISC-V

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RISC-V is a free, open, and extensible Instruction-Set Architecture (ISA) for programmable processor design that is straightforward to implement in many microarchitectural styles [2]. Unlike many earlier efforts that designed open processor cores, RISC-V is an ISA specification, intended to allow many different hardware implementations to leverage common software development. RISC-V is a modular architecture, with variants covering 32/64/128-bit address spaces [2]. The base integer instruction set is lean, requiring fewer than 50 user-level hardware instructions to support a full modern software stack, which enables microprocessor designers to quickly bring up fully functional prototypes and add additional features incrementally. RISC-V comes with several open-source tools, such as a compiler, several simulators, and Linux distributions. Different implementations as soft cores are already available as RTL source code or through code generation [4][5].

In addition to simplifying the implementation of new microarchitectures, the RISC-V design provides an ideal base for building custom accelerators [3]. Accelerators can reuse common processor implementations and they can share a single software stack, including the compiler toolchain and operating system binaries. This dramatically reduces the cost of designing and bringing up custom accelerators. Finally, RISC-V is also suitable for multicore implementation, especially following shared-memory multiprocessor architectures.

In the Inria/Cairn team, we are currently designing an in-order core micro-architecture supporting 32-bit RISC-V instruction set [5]. The Comet core is designed from C++-based specifications using High-Level Synthesis (HLS) tools. The design is compatible with Catapult Synthesis from Mentor Graphics targeting a 28nm CMOS technology library (gate synthesis and validation with Synopsys Design Compiler and Modelsim) and with Xilinx VivadoHLS for FPGA prototyping. Synthesis results obtained through HLS show similar or better performance (clock frequency, area, power, execution time of benchmarks) than other open-source processor core designs [4].

The subject of this work is to extend the Comet processor towards a shared-memory multicore architecture. The main challenge is to deal with C++-based specification of cache memory, on-chip interconnect, protocols for shared memory and multicore specifications. In particular, the research question is how to specify such complex parallel computing pipelines with high-level synthesis technology and to demonstrate that there is a potential high gain in design time without jeopardizing performance and cost (which was the case for the one-core).

In this work, we will also study how some C++-based hardware accelerators (FPU [3], FFT core, approximate arithmetic operators, etc.) can be build and coupled to the RISC-V multicore architecture.

Skills
The recruited person is expected to develop complex processor architectures leveraging C++ and High-Level Synthesis. We also expect to have prototype implementations of the developed techniques on FPGA and ASIC.

Desired skills include:
- Computer architecture, hardware design, VLSI circuit design.
- Basic knowledge in compilers.
- Familiarity with the C/C++ language or other languages.
- Familiarity with FPGA/ASIC design and/or High-Level Synthesis.
- Optimization methods

Mostly importantly, we seek highly motivated and active researchers.

Social advantages
- Subsidised catering service
- Partially-reimbursed public transport
- Social security
- Paid leave
- Flexible working hours
- Sports facilities

Salary - Duration
- 12 to 18 months contract
- Monthly net salary amounting to ~2160 euros

References

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[2] K. Asanovic and D.Patterson, “The Case for Open Instruction Sets,” Microprocessor Report, Aug. 2014.
[3] V. Patil et al., “Out of Order Floating Point Coprocessor for RISC-V ISA,” Proc. 19th Int’l Symp. VLSI Design and Test, 2015.
[4] https://github.com/chipsalliance/rocket-chip
[5] S. Rokicki, D. Pala, J. Paturel, and O. Sentieys. What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications. In 38th IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pages 1–8, Nov. 2019.