Curriculum Vitae

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Olivier Sentieys

Professor, University of Rennes (Univ Rennes)
INRIA Research Chair on *Energy Efficient Computing Architectures*
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Main current responsibilities

- Head, TARAN project-team (formerly CAIRN), joint team with INRIA, CNRS, University of Rennes and ENS (École Normale Supérieure) Rennes. Composed of 11 permanent academic researchers (6 Professors, 2 Ass. Prof., 3 Inria Researchers), 20 PhD students, 3 PostDoc and 5 research engineers.
- Former Head, "Computer Architecture" Department of IRISA Lab. (until Sep. 2019).
- Former Head, "Embedded Systems" branch of the SISEA (Signal, Images, Embedded Systems and Control) Master of Research (M2R) of Rennes University (until Sep. 2021).
- Recipient of Scientific Excellence Award (PEDR, PES) since 1998 without interruption.
- Leader of a French ANR project and participation to several ANR projects, and three European FP7/H2020 projects. Scientific leader of about 30 research contracts and funded collaborations.

Education and Professional Experience

1999	Habilitation, University of Rennes, "Design methods for integrated circuits and embedded systems in the domain of wireless communications".
1993	PhD, University of Rennes, Signal Processing and Telecommunications, "High-level synthesis of VLSI architectures for signal and image: towards the design of heterogeneous multiprocessors".
9/2002 -	Professor, University of Rennes. Promoted to *First Class* Professor (PR1) in 2008 and *Exceptional Class* (PRCE) in 2017.
9/2017 -	Holds the INRIA Research Chair on *Energy Efficient Computing Architectures*.
9/2012 - 8/2017	On secondment at INRIA Research Institute as a Senior Research Director.
9/2017	Promoted to *Exceptional Class* Professor (PRCE).
9/2008	Promoted to *First Class* Professor (PR1).
9/1994 - 8/2001	Associate Professor, University of Rennes I.

Research activities

My research activities are in the complementary fields of computer architecture, computer arithmetic, embedded systems and signal processing. Roughly, I work firstly on the definition of new system-on-chip architectures, especially the paradigm of reconfigurable hardware accelerators, and their associated CAD tools, and secondly on some aspects of signal processing like finite arithmetic effects and digital communications. For more information, see the activity reports of the TARAN team or my web page.

Recent research themes:

- Hardware acceleration for signal, image, machine learning, deep learning and data mining.
- Approximate computing, automatic floating-point to fixed-point conversion, analytical accuracy evaluation, customized arithmetic.
- Energy efficiency, fault-tolerance, and security of computing architectures.
- Ultra-low-power architectures for wireless sensor networks (WSN), energy-harvesting WSNs.

Leadership within the Scientific Community

- Elected member of the Evaluation Committee (CE) of INRIA since 2019.
- Member of the IEEE/ACM DATE Executive Committee (DEC) since 2022.
- Jury member in the EDAA (European Design and Automation Association) Outstanding Dissertations Award (ODA) delivered during DATE Conference since 2016.
- Member of the committee for delivering the Best Paper Award at IEEE/ACM DATE 2020.

- Member of the ANR Scientific Evaluation Committee CE25 "Software science and engineering - Multi-purpose communication networks, high-performance infrastructure".
- Member of the Steering Committee of the SOC2 Expert Group at the CNRS and of the GDR SOC2.

Program committees, editorial boards, conference organization

- Editorial board member of: Journal of Low Power Electronics (since 2006), International Journal of Distributed Sensor Networks (2011–2018).
- Technical Program Committee member of: IEEE/ACM Design and Test in Europe (DATE), 2011–2014, 2016–2022. Co-Chair of the Track on Architectural and Microarchitectural Design at IEEE/ACM DATE (2018–2020). Chair of the Track on Architectural and Microarchitectural Design at IEEE/ACM DATE (2020–2022). International Conference on Field Programmable Logic and Applications (FPL), 2013–. IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2014. ACM Symposium on Integrated Circuits and Systems Design (SBCCI), 2010–. Track Chair, IEEE Northeast Workshop on Circuits and Systems (NEWCAS), 2009–2018. ACM Int. Work. on Energy Neutral Sensing Syst. (ENSSys), co-located with ACM SenSys, 2013–. International Conference on ReConFigurable Computing and FPGAs (ReConFig), 2016–.

PhD Supervisions Supervision or co-supervision of **42 defended PhD Theses**. One is Senior Research Director at CNRS, one Professor (INSA Rennes), eight Associate Professors (ENSSAT, INSA Rennes, ENSICaen, IUT de Lannion, Vietnam, Tunisie, Estonia), four researchers at CEA, and the others are engineers in industry or Postdocs. Supervision or co-supervision of 6 on-going PhD theses.

International collaborations with: University of British Columbia, Vancouver, Canada; University College Cork, Ireland; EPFL, Switzerland; IMEC, Belgique; Québec University at Trois-Rivières, Canada; Laval University, Québec, Canada; University of Massachusetts, Amherst, USA; IIT Goa, India; Tallinn University of Technology, Estonia; Politecnico di Milano, Italy; Universidad Politécnica de Madrid, Spain; Concordia University, Canada; Southeast University, Nanjing, China.
Collaborations with large companies: Kalray, Huawei, Safran, Thales, Nokia Bell Labs, Intel (HARP), STMicroelectronics, Thomson/Technicolor, Alcatel-Lucent, Orange Labs, Atmel, Phillips, Infineon.
Collaborations with SMEs: Temento Systems, Secure-IC, Digidia, PrimeGPS, Feichter Electronics, 3D Ouest, Athemium, Envivio, Geensys, Aphycare Technologies, SmartQuantum, Sensaris, Ditocom, Eca-Faros.
Startup: I was involved in the creation process of a startup around my expertise on automatic fixed-point conversion and error analysis. The company WeDoLow (formerly Yubik) was created in 2022 after an incubation in the Startup Studio of Inria. I am now part of its Advisory Board.

Publications: 4600 citations, h-index=35. Complete list: http://people.rennes.inria.fr/Olivier.Sentieys/?page_id=2 Google Scholar: http://scholar.google.fr/citations?hl=en&user=RYvzLV8AAAAJ.

[FdSKERC+22] Fernando Fernandes dos Santos, Angeliki Kritikakou, Josie Esteban Rodriguez Condia, Juan David Guerrero Balaguera, Matteo Sonza Reorda, Olivier Sentieys, and Paolo Rech. Characterizing a neutron-induced fault model for deep neural networks. *IEEE Transactions on Nuclear Science*, 70(4):370–380, 2023.

[TKS23] Marcello Traiola, Angeliki Kritikakou, and Olivier Sentieys. hardnning: a machine-learning-based framework for fault tolerance assessment and protection of deep neural networks. In *26th IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1–6, 2023.

[PMPS21] Davide Pala, Ivan Miro-Panades, and Olivier Sentieys. Freezer: A specialized nvm backup controller for intermittently-powered systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(8):1559–1572, 2021.

[KPCS20] Angeliki Kritikakou, Rafail Psiakis, Francky Catthoor, and Olivier Sentieys. Binary classification tree of rigid error detection and correction techniques. *ACM Computing Surveys*, 53(4):1–38, 2020.

[BMS22] Alberto Bosio, Daniel Menard, and Olivier Sentieys. *Approximate Computing Techniques: From Component- to Application-Level*. Springer, 2022.

[HS21] Van-Phu Ha and Olivier Sentieys. Leveraging bayesian optimization to speed up automatic precision tuning. In *24th IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1–6, February 2021.

[RPPS19b] Simon Rokicki, Davide Pala, Joseph Paturel, and Olivier Sentieys. What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications. In *38th IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 1–8, Westminster, CO, United States, November 2019. IEEE.

[BSM17] Benjamin Barrois, Olivier Sentieys, and Daniel Menard. The Hidden Cost of Functional Approximation Against Careful Data Sizing - A Case Study. In *IEEE/ACM Design Automation and Test in Europe (DATE)*, page 6, 2017.

[BS17] Benjamin Barrois and Olivier Sentieys. Customizing Fixed-Point and Floating-Point Arithmetic - A Case Study in K-Means Clustering. In *IEEE International Workshop on Signal Processing Systems (SiPS)*, Lorient, France, October 2017.

[HCS15] Christophe Huriaux, Antoine Courtay, and Olivier Sentieys. Design Flow and Run-Time Management for Compressed FPGA Configurations. In *IEEE/ACM Design, Automation and Test in Europe (DATE)*, pages 1551–1554, March 2015.