Architectures and Tools for the Design of Reconfigurable Radio Systems

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Agenda

- What is inside a (reconfigurable) radio system (terminal and base-station)?
- Some challenges
- Reconfigurable architectures
- Design, prototyping and compilation
- On-going and past projects
  - 3G/4G, MIMO
  - Wireless Sensor Networks
- Other research activities
- CAIRN project-team

A cairn in Bréhat
Wireless Communications Systems

- What is inside a radio system nowadays?
  - a hardware platform
    - heterogeneous (GPP, DSP, FPGA)
    - mixed A/D, RF
    - domain or application specific
    - use off-the-shelf and specific components
  - and a lot of embedded software
    - spectrum management, middleware

- Specific constraints
  - Energy and power consumption
  - Cost, re-use
  - Limited resources, real-time
  - Reliability, security

Generic Node Architecture

- Power management
- Digital Processing
- Physical Sensing
- Memory
- Transceiver
- Radio
- Battery
- DC/DC conv.
- Processor
- Coprocessor
- A/D D/A
- Sensor Actuator
- RAM
- Flash
Generic Node Architecture

- **PHY**
- **MAC**
- **LINK**
- **NET**
- **APPLICATION**

**Infrastructure**
- Hardware abstraction, middleware, API

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**Challenges and Limitations**

- **High-performance applications**
  - e.g. 802.11n MIMO, OFDM, WCDMA…

- **Energy and Power constraints**
  - Battery life, manufacturing cost

- **Rapidly changing application standards**
  - SW updates, multi-modes
  - “Software Radio”

- **Technological impacts**
  - Manufacturing reliability issues, transient errors, silicon bugs
A road for reconfigurable chips

“Flexible Software on Flexible Hardware”

- Dynamically adapt the hardware to the application
  - energy-performance-cost trade-off
  - error and fault tolerance
- Self-adapting devices
  - continuously adapt to changing environments

Fresh SoC from CEA with DART
IP from IRISA

Processing Model

RA: Reconfigurable Area
CM: Configuration Management
CAIRN Research Objectives

- Take advantage of CAIRN team skills
  - Compilation, parallelization
  - Architecture, circuit design
  - Signal processing

- to design efficient
  - reconfigurable architectures, multi-mode IP blocks, specialized processors
  - associated compilation or synthesis tools

- for wireless communications (mainly)

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Related Research Themes

- Hardware architectures
  - Dynamic reconfiguration in off-the-shelf FPGA
  - Proposition of new architectures
  - Low-power reconfigurable architectures
- Reconfigurable architecture management
  - On-line scheduling and placement
  - Flexible interconnect
- Compilation from high-level software code
  - Compilation for reconfigurable architectures
  - Floating-point to fixed-point transformations

Reconfigurable Architectures

- Fine-Grain Architectures: FPGA
  - Configurable interconnection array of
    - logic blocks, memory, DSP blocks
    - and processor cores (soft or hard)
  - Complete system on a programmable chip
    - Complex design
- Example: Xilinx Virtex 5
  - 65 nm, 550 MHz
  - 1100 DMIPS PowerPC 440
  - 528 GMACS, 68/192 GFLOPS
  - 1.25 Gbps LVDS I/O
  - Dynamic reconfiguration
Reconfigurable Architectures

- Coarse-grain architectures
  - Reconfigurable data-path
  - Dynamic reconfiguration in a few cycles

- Example: DART (IRISA)
  - 3G/UMTS/802.11a
  - 5-10 GOPS/cluster
  - 300 mW @ 200MHz
  - 16 MOPS/mW @ 5 GOPS
  - Simulator, compiler
  - Fabricated circuit in 130nm

Coarse-Grain Reconfiguration

```c
for (n=0;n<1024;n++){
    tmp=0;
    for (i=0;i<N;i++){
        tmp+=x[i]*h[N-i];
    }
    y[n]=tmp<<6;
    X[0]=x[n]+128;
}
```

- Irregular Processing
  - few parallelism
  - few regularity
  - less complex

- Regular Processing
  - massively parallel
  - very regular
  - complex
Reconfiguration management

Dynamic reconfiguration and allocation of embedded heterogeneous multiprocessor

- Based on neural-networks
  - Scheduling
  - Task placement
- Flexible communication management
- Low-power scheduling policies
- Fault-tolerant approach
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Design and compilation tools

- Goal is to compile from high-level software
  - towards embedded processors
  - towards reconfigurable area
  - to synthesize specific hardware
  - or to extend the instruction-set of a processor
- C to HW tools
  - Source-to-source transformation
  - High-level synthesis
- Dataflow (e.g. Simulink) to HW tools
- Optimization of processing accuracy
Compilation for reconfigurable

- High-level formal transformations
  - Loop parallelization and optimization

- Compilation using complex pattern matching
  - Generation of data-path configurations
  - Automatic extension of instruction-set
  - Constrained-programming optimizations

Accuracy Optimization

- Fixed-point arithmetic
  - Power and cost ↓
  - but more complex design

- Automatic conversion from float to fixed-point
  - Analytical method
    \[
    \min_j [T_{\text{exec}}(WL_j), \text{Cost}(WL_j)]
    \]
    \[
    RSBQ(WL_j) \geq RSBQ_{\min}
    \]
  - *Float2Fix* tool

- Accuracy optimization
  - Optimal structure
  - FWR Matlab toolbox
    - e.g. filtering, control
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Wireless Sensor Networks

- Design of an energy-efficient software stack and hardware platform for wireless sensor networks
- Decrease Tx power
- Optimize radio activity
- Power optimization of the hardware
- Optimize software stack
- Cooperative MIMO/relay
Cooperative MIMO technique

- Three phases of cooperative MIMO communications
  - Phase 1: Local data exchange
  - Phase 2: Cooperative MIMO transmission
  - Phase 3: Cooperative reception

$N_i \rightarrow d_m \rightarrow d \rightarrow N_f$

$\begin{align*}
d_m &< d \\
d_m &\geq 1..10 \text{ m}
\end{align*}$

Energy consumption efficiency

- Cooperative MIMO technique is more energy efficient than SISO and multi-hop SISO techniques for long distance transmission


Rapid Prototyping

- Real-time demonstrators
  - FPGA, DSP
  - Reconfigurable SoC

- WCDMA/3G system (2002)

- MIMO/WCDMA (HSUPA)
  - Flexible hardware architecture
    - modulation, Nyquist filter, spatio-temporal searcher and rake, max-ratio combining
  - Real-time prototype of a WCDMA 2-2
    - From matlab/simulink simulations
    - to real-type prototype
      - base-station, RF front-end, reconfigurable platform

Software Defined Radio (SDR)

- Flexible arithmetic operators
- Multi-mode components
  - Different: modes, parameters, algorithms
  - e.g. channel coding, CDMA
- Adaptive architectures
  - dynamically modify the structure of
    - the architecture, the algorithm, the accuracy
  - depending on the context
    - channel condition, standard, environment
  - e.g. to minimize the dissipated power

Rapid Prototyping for SDR

- GNU Radio for Software Radio
MIMO Systems

- Pre-coding or beamforming
  - Goal: migrate processing towards base-station
  - Linear pre-coder (max-dmin)

- Towards a 4G testbed
  - MIMO/OFDM
    - Influence of algorithmic and precision parameters on the quality of transmission and on energy
  - LTE standard context
  - Suitable for radio-over-fibre


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A cairn in Bréhat
True Random Number Generation

- True Random Number Generator
  - Based on oscillator sampling with random jitter
  - On-chip jitter measurement
  - Embedded statistical tests
  - Suitable for FPGA and ASIC
  - Focus on increasing bit-rate

- MIMO channel emulator
- Collaboration with SmartQuantum
  - Quantum Cryptography

CAIRN team at a glance

- IRISA : Institut de Recherche en Informatique et Systèmes Aléatoires
  - UMR CNRS 6074, INRIA Rennes
  - Nearly 600 people, 31 research teams

- CAIRN team
  - 37 people, Lannion (ENSSAT) and Rennes (Campus de Beaulieu, ENS Cachan)
  - Domain-Specific and Reconfigurable System-on-Chip (architectures, tools, algorithms)
  - Wireless Communications

- Skills in computer science and electronics engineering
  - Compilation, parallelization
  - Architecture, circuit design
  - Signal processing
Summary

- Reconfigurable architecture for wireless systems
- Adaptive and flexible radio architecture
- Power consumption constraints
- Ad hoc wireless sensor networks
- MIMO
- Cooperative/relay