Energy-Aware Computing via Adaptive Precision under Performance Constraints in OFDM Wireless Receivers

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Outline

1. Context and Motivations
2. Energy Consumption Measurement
3. DPS for OFDM Receivers
4. Performance results
5. Conclusions
Low-Power Strategies in Wireless Receivers
• Channel conditions (noise, multi-paths, etc.) are time-varying
• Wireless receivers are designed for worst-case conditions
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- Room for improvement in energy efficiency
  - Signal power (Tx), RF front-end, ADC (resolution), PHY (algorithms, accuracy), FEC performance, etc.
  - BER before FEC between $10^{-2}$ and $10^{-3}$ is usually adequate
- Adaptive transceivers would take advantage of channel conditions
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This work: Adaptive approximate processing in the PHY layer
Fixed-Point Numbers and Arithmetic

Real numbers are represented as scaled integers: \( x = p \times K = p^{-n} \)

\[
2^{m-2} \quad 2^{1} \quad 2^{0} \quad 2^{-1} \quad 2^{-n}
\]

\[
\begin{array}{ccccccc}
S & b_{m-2} & b_{m-1} & b_{1} & b_{0} & b_{-1} & b_{-2} & b_{-n+2} & b_{-n+1} & b_{-n} \\
\end{array}
\]

Integer part \( m \) bits

Fractional part \( n \) bits

\[
\begin{align*}
x &= s \cdot (-2)^{m-1} + \sum_{i=-n}^{m-2} b_i \cdot 2^i \\
s: \text{sign, } m: \text{magnitude, } n: \text{fractional}
\end{align*}
\]

Representation: \((w, m, n)\) with \(w = m + n\)

- Integer part \((m)\): dynamic range
- Fractional part \((n)\): accuracy
Real numbers are represented as scaled integers: \( x = p \times K = p^{-n} \)

\[
\begin{align*}
\chi &= s.(-2)^{m-1} + \sum_{i=-n}^{m-2} b_i.2^i \\
&= s.(-2)^{m-1} + \sum_{i=-n}^{m-2} b_i.2^i
\end{align*}
\]

**Representation:** \((w, m, n)\) with \(w = m + n\)
- Integer part \((m)\): **dynamic range**
- Fractional part \((n)\): **accuracy**

- **Speed-, area-, power-efficient operators** w.r.t. floating point
- But, limited accuracy and low dynamic range
Low-Power Strategies in Wireless Receivers

Reduce receiver performance to save power
⇒ Approximate computing through adaptive fixed-point formats

Performance (BER) can be adapted by tuning word-length $w = m + n$

Loss of accuracy when channel conditions are favorable

A BER of $10^{-2}$ is targeted in this study
Dynamic Precision Scaling (DPS)

Fixed-point formats are chosen at run time according to a metric $p$

Pareto-optimal fixed-point specifications are determined off-line
Contributions of this paper

- Develop a method to implement **low-power DPS** wireless receivers based on OFDM technology (802.11 a/g/n, DVB, DAB, LTE, 802.16)

- **Measure the amount of energy for basic operators** for two architectures (ARM, FPGA), define a cost function, estimate the energy consumed for a fixed-point receiver

- **Propose an estimator** $p$ of the channel conditions (SNR and channel type) to switch between fixed-point implementations
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Goal: Estimate the power consumption of an OFDM receiver ⇒ Compare several fixed-point architectures and compute the energy cost function

Problem: Inaccuracy of power consumption estimation tools (eg. Xilinx Power Estimator/Analyzer)

Solution: Use of an operator library for the required architectures (FPGA, ARM7)
**Goal:** Estimate the energy consumption of *only one* operation, giving the word-length used

**Procedure**

- Specific parallel architecture for each type of operator (adders, multipliers)
- Operator activity analyzed by simulation
- Synthesis, P&R, and power consumption measurement
FPGA - Adders

- Input size $n$
- Output size $n + 1$

Architecture proposition for adders
FPGA - Adders

Results

- Analyzed in Virtex-5 XC5VLX50T, $f = 33\text{MHz}$, $T \approx 30^\circ\text{C}$
- Linear dependency between bit-size and energy
FPGA - Multipliers

Results (DSP)

- Virtex-6
  LX240T,
  \( f = 66\text{MHz}, \)
  \( T \approx 34^\circ\text{C} \)

- Energy can be modeled using piecewise linear functions

\[
\begin{array}{c|c}
\text{w} & \text{DSP operator} \\
\hline
<18 & 1 \\
19 - 25 & 2 \\
26 - 35 & 4 \\
36 - 42 & 8 \\
43 - 48 & 11 \\
\end{array}
\]
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OFDM Receiver and Fixed-Point Model

Receiver model:

- 16-QAM modulation
- FFT size: 512
- Used subcarriers: 300

- CP size: 1/4 FFT
- Frame size: 10 OFDM symbols
- Two channel models: AWGN and Frequency Selective Fading (FSF)
Fixed-Point Selection (off-line)

- Data range and precision evaluated with simulations (for every SNR and channel)

- Intensive simulations made with different precision values

The solution on the Pareto front closer to a BER of $10^{-2}$ is chosen
Energy Consumption Estimation

Partial results

- Up to 74% of the energy can be saved using a DPS algorithm (upper bound)
- $p$ metric determined not only by $\text{SNR}$ but also by channel type
- Low complexity estimator needed
**p-Metric Estimation**

\[ p = f(SNR, \text{channel type}) \]

**SNR**

*Analysis of a Novel Low Complex SNR Estimation Technique for OFDM systems*  
[L. Wilhelmsson et al. 2011]

- **Overhead:** 129 _, 128× , 128+, 1 ÷ (≈ 10 ×)
- **Energy needed:** 25.15nJ

**Channel type**

The equalizer coefficients (calculated for equalization) provide a good estimator of the channel type

- **AGWN:** flat coefficients
- **FSF:** irregular coefficients

\[ \hat{\phi} = \sum_{i=nk}^{N/k} \left| eq_i^2 - e_{eq}^2 \right| \quad n = 1, 2, ... \]

- **Overhead:** 2N/k ×, 2N/k +, 2N/k −, 1 ÷ (≈ 10 ×)
- **Energy needed:** 8.7nJ  
  (12 bits, N/k = 32)
• Reduce receiver performance when BER is below $10^{-2}$
Total overhead
- \(385 \pm 192 \times, 2 \div (\approx 20 \times)\)
- Compared with FFT: 2.96% \(\pm\), 2.8% \(\times\)
- Static cost of estimator (12 bits): 32nJ

Energy saving: 63% (maximum)

Guaranteed performance even with wrong channel estimations
Conclusions and Perspectives

Conclusions

- Power savings can be achieved in an OFDM receiver using adaptive word-length without modifying the original OFDM frame
- SNR and channel type estimators are good and cheap
- FPGA: a maximum gain of 63% (using our estimator)
- ARM 7 TDMI: a maximum gain of 34% (details are in the paper)

Perspectives

- Influence of extra blocks in the receiver (channel estimation, synchronization) should be analyzed
- Long off-line simulations: analytic or hybrid methods for word-length exploration
- Much better gains are expected for ASIC designs
References

FPGA - Multipliers

Results (no DSP)

- Analyzed in Virtex-5 XC5VLX50T, $f = 33\text{MHz}$, $T \approx 30^\circ\text{C}$
- Modeled as $C(w) = a \, w^b$
During calculation, four operations made:

- LDR R4, [R0], #offset
- LDR R5, [R1], #offset
- ADD R0, R4, R5
- STR R0, [R6], #offset
ARM 7 TDMI

Adders

Dynamic energy consumption of adders (ARM7TDMI)

- Constant word size (32 bits)
- \( \lim_{w \to 0} C(w) \neq 0 \)
- Similar values \( \Rightarrow \) High cost of LDR and STR

Multipliers

Dynamic energy consumption of multipliers (ARM7TDMI)

Experimental data
Linear Regression \( (r = 0.99459) \)

Experimental data
Approximation \( (\sqrt{EQM} = 11.2851) \)