Some opportunities for energy reduction in WSN

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Wireless Sensor Networks (WSN)

- Dense network of small nodes communicating through wireless links
  - for sensing, actuation, communication and control
  - on-demand or event-driven models
- Simplified deployment, fault tolerance
  - Ad hoc network
- Network characteristics
  - Low mean distance
  - Limited amount of data
  - Multi-hop routing
- Low cost
- Long autonomy
Wireless Sensor Networks

- Tremendous space of applications
  - Monitoring space: ocean water, pollution,
  - Monitoring things: robots, human body,...
Great Duck Island

- 150 sensor nodes
Zebra Net

- Zebras equipped with GPS collars
Volcano monitoring

Phenomena whose monitoring discourages human presence are best observed with WSNs.

Harvard, Univ. of New Hampshire, Univ. of NC
ANR SurVeiller et Prévenir

- Capteurs de paramètres physiologiques
  - Suivi de l’activité physique
  - Prévention de l’obésité
- [http://svp.irisa.fr](http://svp.irisa.fr)
Captiv

Cooperative wireless communications
ITEA2 Geodes: fire-fighters

- Indoor network
  - Temperature monitoring, smoke detection, motion detection
  - Camera nodes

- Mobile nodes (fire-fighter)
  - Health monitoring, camera, etc.
  - Connected with indoor network
Generic architecture of a wireless node

- Generator
- Battery
- DC/DC conv.
- Sensor
- A/D
- Processor
- Coprocessor
- RAM
- Flash
- Radio
Generic architecture of a wireless node
Main Goals

- *How to design and optimize an energy-efficient software and hardware platform for wireless sensor networks?*

- (1) Decrease transmission (Tx) power
- (2) Optimize radio activity and MAC
- (3) Power optimization of the hardware
- (4) Optimize software stack
Agenda

- Node architecture
  - HW Platform
  - SW Stack
  - Platform and network simulation

- Energy optimization (1)
  Question is “How much (signal) processing can I add to reduce the radio Tx/Rx power in order to optimize the global energy (or autonomy) of the network?”
  - Cross-layer (MAC/LINK)
  - MIMO Cooperation

- Energy optimization (2)
  - FPGA co-processing
  - Architectural and Circuit Level Optimization
WSN HW Platform (2008)

- Modular board design
  - Mother board MSP430
  - Daughter board for
    - CC2420
    - FPGA
    - Sensors
    - DVFS

- Microprocessor
  - TI MSP430
  - Fclk: 5 MHz
  - Valim: 2.7 - 3.6 V
  - RAM/Flash: 5 Ko/55 Ko
  - 500uA/MHz@3V
  - 330uA/MHz@2.2V
  - Low Power Modes
    - 50uA, 11uA, 1.1uA, 0.1uA

- Radio transceiver
  - TI CC2420
  - 802.15.4/ZigBee compliant
  - Frequency: 2.4 GHz
  - Sensitivity: -95 dBm
  - Max rate: 250 Kbits/s
  - Chip rate: 2 Mchips/s
  - PTx: 25 dBm to 0 dBm
  - Tx Power 17.5mA at 0 dBm
  - Rx Power 18.8mA
  - Idle/Down 426uA/20uA

PowWow: Power optimized hardware/software frameWork for Wireless motes
Chipcon Radio Transceivers

![Graph showing power consumption vs. emitted power for different models. The graph illustrates the relationship between current consumption in mode Tx and emitted power in dBm for Chipcon models CC1020, CC2420, Location, and NorthWest.]
PowWow SW Stack

- Open source software developed at IRISA/CAIRN
  - [http://powwow.gforge.inria.fr](http://powwow.gforge.inria.fr) (June 2009)
- Based on Protothread library and Contiki
  - Event-driven programming
  - Flexibility, compactness of code
- HAL, PHY, LINK, MAC, NETW, API
  - FEC/ARQ, geographical routing, positioning, Tx power management.
  - Modes: broadcast, flooding, direct/multi-hop with/without ACK
  - Configurable packet structure
- Memory efficiency
  - 6 Kbytes (HAL-NETW) + 5 Kbytes (APPLICATION)
- Analytical power estimation based on software profiling and power measurements of a set of scenarios
- Over-the-air re-programmation (and reconfiguration)
Platform simulation: WSim+WSNet

- Open source software developed at INSA Lyon
- WSim: hardware platform simulation
  - Cycle accurate simulation
  - Several models (processors, transceivers, peripherals)
  - Interaction with WSNet for distributed network simulation
  - Application final binary
- WSNet: event-driven simulator for wireless networks
  - Node simulation
  - Environment simulation
  - Radio medium simulation
  - Extensibility
- [http://wsim.gforge.inria.fr](http://wsim.gforge.inria.fr)
- [http://wsnet.gforge.inria.fr](http://wsnet.gforge.inria.fr)
Power optimization of a wireless node
MAC layer

- MAC layer
  - Asynchronous RDV scheme initiated by receiver
  - RICER (Receiver-Initiated CyclEd Receiver) [Lin05]
Power Measurements on PowWow HW

- Wake-up and channel sensing

All measurements realized with Agilent N6705A DC Power Analyzer
Power Measurements on PowWow HW

- Wake-up and channel sensing

6, 8, 16, 32, 64, 128 packet size in bytes
Power Measurements on PowWow HW

- Wake-up and channel sensing with collision
Results on MAC parameter optim.

- Wake-up period influence

- Short WUP
  - 0.2 s
  - 19.45 mW
  - 19.3 Days

- Optimal WUP
  - 1.6 s
  - 5.64 mW
  - 66.5 Days

- Long WUP
  - 8.0 s
  - 12.17 mW
  - 30.8 Days

Legend:
- Transmission Mode
- Receiver Mode
Power optimization of a wireless node
Performance/energy joint modelling

- Energy per successfully transmitted bit

![Graph showing energy per successfully transmitted bit vs. transmission power for CC1020 transceiver.]

\[ E = \frac{x}{N} \]

\( D = 10 \text{ m}, P_{\text{noise}} = -90 \text{ dBm}, 53 \text{ bytes packets} \)

CC1020 transceiver

Power optimization of a wireless node
HW Platform Energy Optimization

- (1) Co-processing
- (2) Dynamic Voltage Scaling
- (3) Power Gated FSM
- Dynamic Precision Scaling, etc.
Coprocessing with Low Power FPGA

- **Actel Igloo FPGA**
  - AGL125, 130nm, 125k gates
  - 32kbits RAM, 1 kbits Flash, PLL
  - 1.2V (0-1.65V)
  - 2.2uW/16uW/1-30mW (sleep/freeze/run)
  - Implemented Viterbi for link layer: 5mW

- **FPGA power efficiency on CRC32**
  - CRC32 on MSP430
    - $E_{msp} = 150 \mu s \times 20mW = 3\mu J$ (at 8MHz)
  - CRC32 on Actel Igloo AGL125
    - 125k gates, 36kbits RAM,
    - $E_{igloo} = 0.8\mu s \times 5mW = 0.004\mu J$ (at 20MHz, including I/O)
    - Energy saving $= 150/0.8 \times 20/4 = 750$
Dynamic Voltage Scaling (1/3)

DVS (and frequency)
1.6V, 1.8V, 2V, 2.5V, 3V, 3.3V
Dynamic Voltage Scaling (2/3)

Power of MSP430

1.6V, 1.8V, 2V, 2.5V, 3V, 3.3V

\[ P \propto V_{dd}^2 \]
Dynamic Voltage Scaling (3/3)

Power of MSP+CC2420

1.6V, 1.8V, 2V, 2.5V, 3V, 3.3V

\[ P \propto V_{dd} \]
Power Gated Controllers (1/3)

- Power Gating Principle

![Diagram of Power Gated Controllers]

- Power Gating Principle

![Diagram of Power Gated Controllers]
Power Gated Controllers (2/3)

- Task graph to gated FSM

(a) System level view of an application mapping
Power Gated Controllers (3/3)

- Power gain versus MSP430 software execution

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<th>Gain (x)</th>
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TABLE I

SUMMARY OF DYNAMIC POWER CONSUMPTION FOR VARIOUS TARGETS.

- LGSynth’93 Benchmark FSM
- Randomly generated FSM

Power optimization of a wireless node
Cooperative MIMO using STC for WSN

- MIMO space-time coding => Diversity gain
  - Reduces the error rate or transmission energy
- In WSN: Limited size or limited cost of each wireless sensor node
  - Each node can support only one antenna
  => Direct application of MIMO transmission technique is difficult

Individual nodes can cooperate

Cooperative MIMO technique

- Diversity gain of MIMO STBC
  - Energy efficiency of MIMO technique for long range transmission
Cooperative MIMO technique

- Three phases of cooperative MIMO communications
  - Phase 1: Local data exchange
  - Phase 2: Cooperative MIMO transmission
  - Phase 3: Cooperative reception

\[ \text{S} \quad \text{d} \quad \text{MIMO transmission} \]
\[ \text{d}_m << \text{d} \]
\[ \text{d}_m = 1..10 \quad \text{m} \]

\[ \text{d}_m \quad \text{N}_t \quad \text{N}_r \]

Colloque GDR SoC-SiP, 10/6/2009
Energy consumption of cooperative MIMO

- Cooperative MIMO technique is more energy efficient than SISO and multi-hop SISO techniques for long distance transmission [1,2]


Summary

- Energy minimization in WSN
  - Complex cross-layer problem
  - Power/performance models

- Reduction of Tx Power
  - Signal processing, error correcting code

- Reduction of Rx activity
  - MAC, routing

- Power optimization of heterogeneous platforms
  - Power management, dedicated hardware, power gating, etc.

- Power optimization of analog and radio
Design challenges

- Computer Science
  - Verification
  - Distributed computing
  - Embedded software
  - Middleware
  - Operating Systems
  - Micro-architecture
  - CAD tools
- Microelectronics
  - Digital
  - Analog
  - RF
- Communications
  - Modulation
  - MAC
  - Routing
  - Channel coding
  - MIMO, relay
- Signal Processing
  - Hybrid systems
  - Networked control
  - Source coding
  - Channel coding
  - MIMO, relay
- Control
- WSN
  - Hybrid systems
  - Networked control
  - Source coding
  - Channel coding
  - MIMO, relay

energy consumption
Questions ?
**Perpectives**

- PowWow Version 2 includes
  - FPGA for low-level processing and hardware acceleration
  - Voltage scaling
  - Wake-up for ultra-low-power modes
Bibliography