MVL circuit design and characterization at the transistor level using SUS-LOC

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Abstract

This paper deals with design and performance estimation of typical ternary functions using SUS-LOC concepts. Experimental models of the transistors needed for SUS-LOC structures are presented. A created characterization process allows to extract the delay and the energy consumption information from each cell which is simulated at the transistor level. Finally, VHDL is used to obtain performances modelling and architectural-level simulation. Some characterization results are presented for basic logic ternary functions and a comparison between binary and ternary circuits is given for two adder structures.

1. Introduction

The performances of Very Large-Scale Integrated circuits (VLSI) are limited by complex wiring (a great amount of the chip performances is devoted to interconnections), large propagation delay and high power consumption. Several research orientations relate to the improvement of these performances and one of them is the Multiple Valued Logic (MVL) [4]. Thus, the first question is: does the design in MVL can allow to obtain better performances for VLSI circuits? Obviously the best way to know is to design and characterize an MVL circuit and to compare it with its binary equivalent. But the second question is: how to implement efficiently MVL circuits? Many technologies have been considered to implement MVL circuits like bipolar technologies (Integrated Injection Logic (I^2L) or Emitted-Coupled Logic (ECL)), Current-Mode CMOS Logic (CMCL) [10, 11, 6, 3]), Voltage-Mode nMOS technology [13], CCD technology [2], and Quantum Functional Devices (QFD) technology [1]. In spite of advantages due to MVL, mainly the reduction of interconnections, these technologies have for the moment severe disadvantages, which prevent them from replacing existing binary circuits. A disadvantage of CMCL circuits is the high consumption induced by the static currents corresponding to logic states. Surface-CCD binary circuits have their speed limited to low frequencies [2]. QFD devices are not at a mature stage yet. Voltage-mode circuits with multiple thresholds for each transistor have high design cost [12].
In this paper, new concepts for MVL design are considered. The SUpplementary Symmetrical LOgic Circuit structure (SUS-LOC) presented in [8] is a new approach for the implementation of MVL functions in voltage-mode. The SUS-LOC concept has been validated at the register-transfer level in [9]. This paper presents its validation at the architecture, logic and transistor abstraction levels. If, for binary circuits, there are available transistor model cards and Computer-Aided Design (CAD) tools that allow to run these validations, it remains that, for MVL circuits, there is the need to have specific model cards for the required transistor types for the SUS-LOC and specific tools for ternary circuit design and characterization. We propose a methodology and some CAD tools dedicated to the performance (delay, power) estimation of MVL voltage-mode structures and present some characterization results.

The section 2 exposes transistor models required for SUS-LOC and how fast estimation of cell energy consumption can be obtained. The section 3 presents the obtained results on some ternary cells such as the inverter and the CGAND function and on two adder structures which are the Ripple Carry Adder (RCA) and the Sklansky adder. Delay and energy comparison between binary and ternary are given for these structures.

2 Design and characterization of ternary cells using SUS-LOC

2.1 Transistor library

Specific transistors are needed to implement the SUS-LOC concepts due to their different threshold voltages (V_{th}). For instance, the table 1 shows an example of a list of transistor types with their respective V_{th} needed for the SUS-LOC implementation. The threshold voltages are

given for enhancement (ENH) and depletion (DEPL) transistors and for two kinds of power supply ($V_{dd} = 2.5V$ or $2.0V$) that we used for two different technologies. Firstly, the results that are given in this paper are extracted from a 0.25μ bulk CMOS technology with $V_{dd} = 2.5V$ and logic state voltages of respectively $\{0V, 1.25V, 2.5V\}$. The experimental transistor model cards used for all the circuit simulations are derived from the level 3 model of SPICE. The figure 1 shows the obtained $Id(V_{gs})$ curves for each transistor. The circuit simulator that was used is ELDO from Mentor Graphics Corp. A second technology has been considered in order to be able to fabricate a prototype chip soon. In this case, we use an SOI (Silicon On Insulator) CMOS technology from UCL (Université Catholique de Louvain-La-Neuve) with $V_{dd} = 2.0V$ and logic state voltages of respectively $\{0V, 1V, 2V\}$. Using this SOI technology, the different transistors, especially the depleted ones, can easily be fabricated by acting on doping parameters and the performances in term of energy efficiency will be improved in regard to bulk CMOS [5].

2.2 Performance modelling and architectural-level simulation

All designed cells have been characterized in delay/power with the LUT (Look-Up table) method which considers the global energy evaluation and the delay propagation for a given standard load. As the cell energy consumption depends on the input transitions, the transitions of M-inputs cells can be modeled like a $2.M$-tert word, with M integer and $M \geq 1$, taking into account previous and current states of the inputs. A tert is defined as a ternary digit which can take the states $\{0, 1, 2\}$. Specific tools have been developed in order to take account of the specific features of ternary logic. The corresponding characterization flow is presented in the figure 2. XCircuit (XCircuit Reference Manual is available from the link http://xcircuit.ece.jhu.edu/) and MVLStim, which is a developed C-program that generates input stimuli vectors, are used for an easy cell netlist description (the hierarchical netlist). The transistor-level simulation results under ELDO

Table 1. Threshold voltages of the transistors

Transistor Type	Mode	V_{TH} (V)	
		$V_{dd} = 2.5V$	$V_{dd} = 2V$
PMOS(P+)	ENH	-1.625	-1.3
NMOS(N+)	ENH	1.625	1.3
PMOS(P)	ENH	-0.375	-0.3
NMOS(N)	ENH	0.375	0.3
PMOS(PD)	DEPL	0.875	0.7
NMOS(ND)	DEPL	-0.875	-0.7

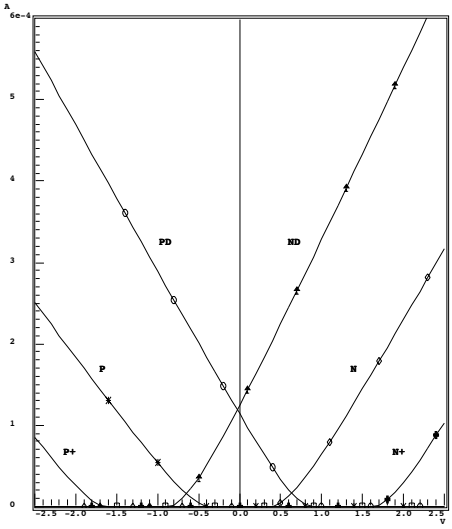

Figure 1. $Id(V_{gs})$ characteristics of the MOSFETs

are input data for MVLCara which is another developed C-program that extracts from SPICE simulation results the delay and the energy consumption corresponding to each input transition. The cells can be automatically characterized with MVLCara after circuit simulation and a report file that will be used during VHDL gate-level simulations is generated.

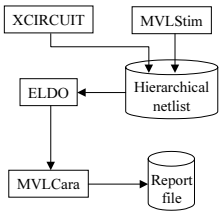

Figure 2. Characterization process flow

The first step in the VHDL modelling consists in the installation of a ternary environment. We defined new VHDL types (*TERT* and *TERT_VECTOR*) and new ternary functions. For instance the *TERT* type is defined as:

```
-- logic 3-state unresolved type
TYPE TERT IS ( 'X',  -- Forcing  Unknown
               '0',  -- Forcing  0
               '1',  -- Forcing  1
               '2',  -- Forcing  2
               'Z'   -- High Impedance
                );
--resolution function
function resolved_3 (s : TERT_VECTOR) return TERT;
SUBTYPE rTERT IS resolved_3 TERT;
```

Some of those functions are overloaded predefined functions of standard packages so they can be used with the new

ternary variables. The second step is the modelling of a ternary cell taking into account the delay and the energy consumption parameters. The VHDL modelling process of a cell is made according to the diagram of the figure 3. The delay and energy consumption information are stocked in tables (as time or real type vectors) in a package.

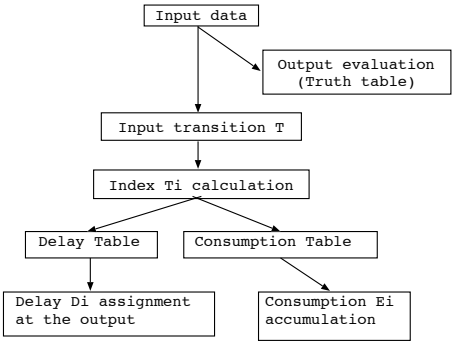

Figure 3. Synoptic diagram of the behavioral description of a cell.

The third step is the generation of the test vectors and the calculation of the propagation delay and the total energy consumption after VHDL gate-level simulations. For instance for the VHDL model of the CGAND cell, the following descriptions are for the delay and the energy consumption evaluation during simulation.

```
param := (0=>lastB, 1=>lastA, 2=>B, 3=>A);
delay := delay_func(param, Tab_delay);
energy :=  energy_func(param, Tab_energy_v1)+
          energy_func(param, Tab_energy_v2);
cal_energy := cal_energy + energy;
total_energy <= cal_energy;
```

The present values on the inputs of the CGAND cell are A and B and the past values, lastA and lastB. For instance if A=B=1 and lastA=lastB=2, then param=2211 identifies the transition. Tab_delay, Tab_energy_v1 and Tab_energy_v2 are arrays which contain energy consumption due to V1 and V2 and delay data arranged by transition. Finally the delay and the consumption are evaluated with delay_func and energy_func functions, and the consumption is updated in the *total_energy* variable. We opted to make VHDL simulation with series of 10^4 pseudo-random test vectors. For a complex block (e.g. the adder of figure 10), the total energy consumption is the sum of cell energy consumption occurred for every transition. This method enables to take the dynamic hazards (i.e. glitches) due to propagation delays of the gates into account when estimating power, and is the equivalent in ternary with classical gate-level simulation and power estimation that can be used for binary circuits (e.g. Synopsys Design Power).

3 Ternary cell design

Some ternary cell design and characterization are presented in this section. The first considered ternary cell is the inverter which is characterized and compared with a binary inverter. Then, the CGAND cell and two adder structures are considered.

3.1 The ternary inverter

The figures 4.a and 4.b represent respectively a binary and a ternary inverter with their corresponding truth table.

The well known CMOS binary inverter is created with

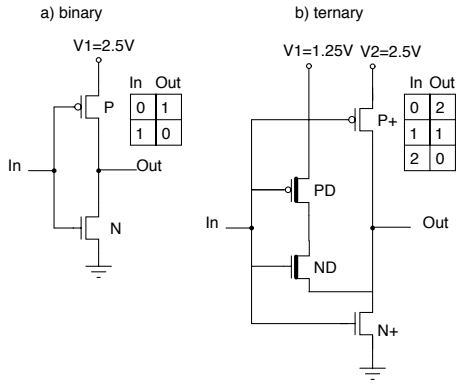

Figure 4. Binary and ternary inverters

enhancement transistors (P and N). According to [8], the ternary logic is implemented with enhancement transistors (P+ and N+) and depletion transistors (PN and PD). Enhancement transistors can have two different threshold levels. Thus for binary benchmark cells we have two alternatives, either we use a high threshold level (named here HTL) or a low threshold level transistor (named here LTL). This respectively corresponds to low-power or high-speed transistors.

For the ternary structure, the pull-up (P+) and the pull-down (N+) network is common with the binary one. The *pull-one* network, which allows to transmit the state 1 (i.e. 1.25V), is represented by PD and ND. By carrying out an energy and a delay analysis between HTL and LTL binary inverters and the ternary one, we can highlight advantages and drawbacks. For example, we can study slow ramp effects which deteriorate delay and power performances in CMOS cells. While varying the slope duration from 100ps to 400ps, we measure the energy consumption and the delay propagation reported respectively in the table 2 and 3. For all the results of the section 3, we consider a capacitive load of 5fF for the binary and of 8fF for the ternary. The energy consumption is measured by taking into account only the flowing out current of generators. Delay is measured at

time when input and output pass by $V2/2$ for radix 3 and $Vdd/2$ for radix 2 for a $0 \rightarrow 2$ transition. For the ternary inverter the given results are for an output transition from 0 to 2 and from 0 to 1.

Table 2. Energy measuring [fJ]

Inverter	Input slope[ps]				
	100	150	200	300	400
Binary HTL	66.9	67.5	67.5	67.4	67.5
Binary LTL	69	73	76.8	83.7	90
Ternary ($0 \rightarrow 2$)	78.6	77.5	75.8	74	72.6
Ternary ($0 \rightarrow 1$)	29.3	30.9	30.1	30.6	30.6

Table 3. Delay measuring [ps]

Inverter	Input slope[ps]				
	100	150	200	300	400
Binary HTL	168	185	202	237	272
Binary LTL	62.8	73.5	83.1	100	117
Ternary ($0 \rightarrow 2$)	133	134	138	154	237
Ternary ($0 \rightarrow 1$)	138	143	149	162	176

LTL configuration, currently used for binary purposes provides a higher charging or discharging current than HTL transistors, because the current capabilities depend on $Vgs - Vth$. This causes the lowest delay propagation for binary LTL. But, as the threshold is low, it exists a range where pull-up and pull-down network conduct at the same time causing short-circuit current from power supply to ground with a voltage that yields the short-circuit at V1=2.5V. This happens on binary cell when the slope duration becomes bigger than the delay propagation. On ternary structures, short circuit happens on pull-up and pull-one or on pull-one and pull-down. Thus, the short-circuit current is less important than binary one because there are more channel-connected elements for a smallest short-circuit voltage at 1.25V ($V2-V1$ or $V1-0$). Moreover, we can notify that ternary is faster than HTL transistors even with the same common structure. This is caused by the pull-one network which starts yielding the loading capacitance before the pull-up network. For greater slope duration, energy consumption is decreasing for ternary inverter because the more the input slope is slow, the more the transistor ND is OFF before P+ becomes ON. Finally between standard CMOS circuits designed with LTL transistors and SUS-LOC circuits, the delay variation for these four slope durations is lightly less important than for the SUS-LOC inverter. Moreover, the energy consumption remains ranging between 70fJ and 80fJ, which gives us a variation of -7.6%, while for the LTL inverter, the variation reaches 30.4%.

3.2 The CGAND function

Another basic function is the CGAND (Complementary Generalized AND). The figure 5 shows an example of a switch diagram for the CGAND (Complementary Generalized AND) function defined as the inverse of the minimum between two inputs:
$CGAND(x,y) = N(MIN(x,y)),$ with $x,y \in \{0,1,2\}$
and the figure 6 presents the translation of the switch diagram into a netlist of transistors realizing the CGAND function. The network for $V2$ and $V0$ are similar to those used in binary CMOS, and the network providing the $V1$ voltage level uses depleted and enhanced MOS transistors and is specific to SUS-LOC. The simulation results presented in

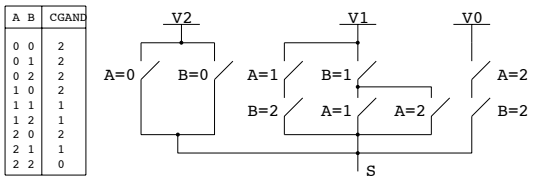

Figure 5. The switch diagram of CGAND

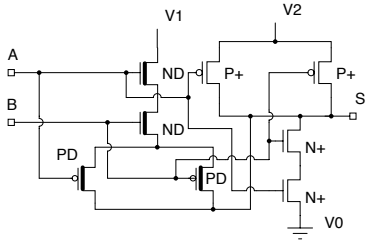

Figure 6. The schematic of the CGAND

the figure 7 correspond to the truth table of the inverted min function, implemented by the CGAND cell. From the simulation result file, we have extracted the delay and energy information for each input transition. The critical delay and the maximum energy consumption by input and output transitions, obtained in sub-optimal conditions, are given in the table 4. The full characterization table contains up to 81 different transitions for a 2-place ternary function. The table 4 gives in the first line the transition corresponding to the maximum value of the propagation delay on all transitions, while the second line gives the maximum value of the consumed energy. The mean value of the energy for all transitions is equal to 21 fJ. This value for the CGAND is in the same order of magnitude than the mean energy of a binary NAND gate (15.8 fJ), but for a more complex logic function.

Table 4. CGAND characterization

Input Transition	Output Transition	Delay	Energy
$00 \rightarrow 11$	$2 \rightarrow 1$	500 ps	0.8 fJ
$22 \rightarrow 00$	$0 \rightarrow 2$	200 ps	151 fJ

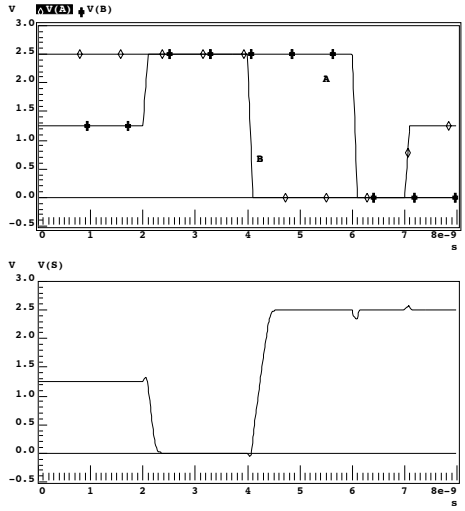

Figure 7. The CGAND simulation results

3.3 Ternary adders: RCA and Sklansky structures

A key element of a DSP is the arithmetic unit, and the question is about the evaluation of energy consumption of ternary adders and their comparison to the binary ones. After consideration of the classical Ripple Carry Adder (RCA) structure, we focused on an optimized structure: the Sklansky structure. The synoptic diagrams of the RCA structures on 40 bits and on 25 terts are given on the figure 8. The Full

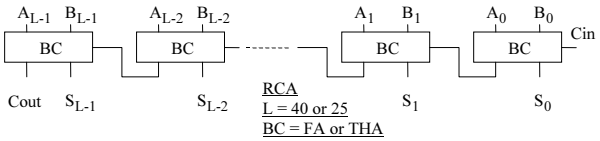

Figure 8. Synoptic diagrams of 40 bits and 25 terts RCA structures

Adder (FA), defined as:

$FA(A_i, B_i, Cin_i) = (Z1, Z0) = A_i + B_i + Cin_i$,

is the basic cell for the binary adder. The Ternary Full Adder(TFA) is defined as:

$TFA(A_i, B_i, C_i, Din_i) = (Z1, Z0) = A_i + B_i + C_i + Din_i$,

where $Z0$ is the sum modulo 3 of A, B, C and Din, and $Z1$ the output carry. But for the design of a ternary RCA, a basic adder cell, called Ternary Half Adder (THA) and defined as:

$THA(A_i, B_i, Cin_i) = (Z1, Z0) = A_i + B_i + Cin_i$,

is sufficient. It has only 3 ternary input data A_i, B_i, Cin_i with Cin_i taking only the values 0 or 1.

As the optimized structures of adders are based on the principles of generation (G_i) and propagation (P_i) [7], it was necessary to extend these principles to ternary logic. The ternary P_i and G_i are defined as: if $A_i + B_i \geq 3$ then $G_i = 1$, else $G_i = 0$, and if $A_i + B_i = 2$ then $P_i = 1$, else $P_i = 0$. The Sklansky adder structure is similar to the binary one, except for the P_i and G_i cells and for the addition modulo 3 block at the output named Sum bit/tert Computation (see the figures 9 and 10). On the figures 9 and 10, the $\triangle$ operator represents the binary Brent and Kung (BK) cell which is defined as [7]: $BK((G_2, P_2), (G_1, P_1)) = (G_3, P_3)$, with $G_3 = G_2\ OR\ (P_2\ AND\ G_1)$ and $P_3 = P_2\ AND\ P_1$. As ternary P_i and G_i are also binary functions, the same binary BK cell can be used for the ternary Sklansky adder too. The table 5 presents the critical delay and the number of transistors of each structure, and the table 6 summarizes the VHDL energy consumption estimation results. The Sklansky adder is the most interesting since it consumes 2 times less energy than its binary equivalent. For larger data size (e.g. 64 bits vs. 40 terts), ternary will continue to obtain far better performances with a transistor-count equivalent to that of the binary structures.

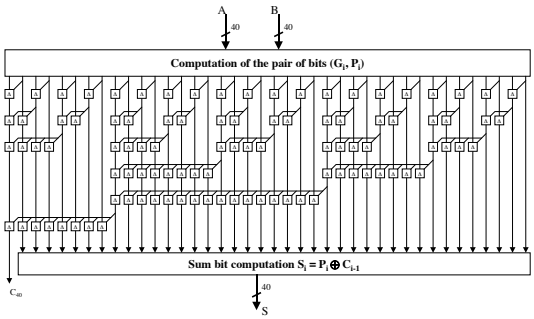

Figure 9. A 40 bit sklansky adder structure

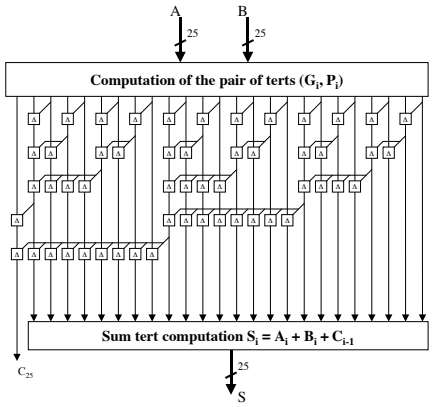

Figure 10. A 25 tert sklansky adder structure

Table 5. RCA and Sklansky adders critical delay (picoseconds) and number of transistors

BINARY	RCA	$Sklansky$
Delay(ps)	19000	4421
Transistors	1440	3680
TERNARY	RCA	$Sklansky$
Delay(ps)	26250	4675
Transistors	2175	4296

Table 6. Energy consumption (in nano-Joules) for RCA and Sklansky adders

BINARY		TERNARY	
RCA	$Sklan.$	RCA	$Sklan.$
348.03	536.94	399.72	190.40

3.4 Other functions

To provide a basic ternary standard-cell library, the following functions have been also designed and characterized at the transistor level.

- Inverter function $N(x) = \langle 210 \rangle$
- $C_0 = \langle 200 \rangle, C_1 = \langle 020 \rangle, C_2 = \langle 002 \rangle$: $C_i(x) = 2$ if $i = x$ and $C_i(x) = 0$ if $i \neq x$ with $(i, x) \in \{0, 1, 2\}^2$
- $CGOR(x, y) = N(MAX(x, y))$, with $x, y \in \{0, 1, 2\}$
- 2-input multiplier $M(x, y) = x \times y$, with $x, y \in \{0, 1, 2\}$
- 2-input multiplier with carry input $M'(x, y, C_{in}) = (x * y) + C_{in}$, with $x, y, Cin \in \{0, 1, 2\}$
- Ternary half adder $THA(x, y, Cin) = x + y + Cin$, with $x, y \in \{0, 1, 2\}$ and $Cin \in \{0, 1\}$
- 2- or 3-input multiplexers, transmission gates, D latch, D flip-flop, ...
- SRAM (Static Random Access Memory) basic cell, address decoder for memory access.

4 Conclusion

In this paper, we have presented how the SUS-LOC concepts can be applied for the design of ternary functions at the transistor level. We used metrics like delay, energy consumption and transistor cost in order to perform comparison between ternary and binary circuits. Estimation results on cells, such as the inverter and the CGAND, or on sub-modules, such as adders showed globally that it could be interesting to invest in a layout abstraction level validation of SUS-LOC concepts. For complex arithmetic structures (e.g. Sklansky adder), we showed that the consumed energy can be divided by two compared to its binary equivalent, for a similar delay.

Our work is currently focusing on the design of a ternary DSP core, especially on the processing and SRAM memory unit. The considered processing unit needs sub-modules like shifter, register, multiplier, multiplexer, adder and ALU. All components of this DSP core have been designed at the transistor and gate levels and useful performance comparisons are made between radix 2 and radix 3 logics. These predictions about energy and delay performances are very encouraging for the continuation of our study on a DSP implementation with SUS-LOC structures. The next validation step is the design at the layout level using an SOI technology from UCL.

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