# On-chip interconnects energy consumption: High-level estimation and architectural optimizations

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## 1. Thesis abstract

Nowadays, applications are more and more complex and require many computational resources, which involve a large amount of data to be stored or translated from a unit to another. Moreover, with technological parameters evolution, controlling propagation time and power consumption of *SoC*'s interconnects becomes a major issue. *ITRS*'s predictions show wire and transistor dimensions shrinking, which imply circuit behaviour modification; especially with propagation time (the wire propagation time is higher than the gate one). This increase is among other things, due to the increase of interconnect's resistance and capacitance. These increases also involve a power consumption growth due to interconnects which can represents up to 50% of the whole chip power consumption. So it is now necessary to take interconnect's power consumption into account during the chip power consumption evaluation.

Based on these facts, our work has been developed in four steps. First, a complete physical interconnects modeling has been proposed. Then, according to these models, *SPICE* experiments allowed us to develop a power consumption estimation tool (*Interconnect Explorer*). The tool has been used to characterize the impact of the state of the art optimization techniques in a third step. Based on this study, some new key issues for power consumption optimization have been proposed. Finally, some new optimization techniques according to the new issues have been developed. In the following of this abstract, each of the steps will be presented in more details.

Our work has first focused on physical bus modeling for power consumption [3]; distributed resistance and capacitance wires have been characterized. Then, from a bus point of view, buffer and crosstalk capacitances have also been considered. Power consumption impacting parameters (technology, metal layer, bus length...) have been extracted thanks to *SPICE* simulations of the circuits. Experimental results, provided by the simulations, allowed us to realise energy/power models which have been included in our estimation tool.

Our tool (*Interconnect Explorer*) allows users, after configuration step (technology, metal layer, bus length choices for instance) to obtain rapidly power/energy consumption estimation of the data bus transfer. Validation experimentations show that the maximum error of *Interconnect Explorer* is 3% compared to *SPICE* simulations and requires only a few seconds compared to few hours with *SPICE* in the same experimental conditions.

Then, a state of the art of the major power and timing optimization techniques has been realized [3]. The estimation tool allows us to validate the techniques efficiency on the power consumption. The analysis of the results, provided by *Interconnect Explorer*, demonstrates that optimization techniques do not face the good criteria. For instance, the propagation time transition classification is different from energy point of view. This means that techniques aiming at suppressing worst propagation time transition, by doing the hypothesis that these transitions are also the worst for energy, are not as efficient as they should be. Moreover, many of the proposed methodologies have a quite high material overhead, particularly due to their codecs. These codecs leads to power consumption overhead often higher than the power consumption reduction they can lead on the bus for usual *SoC* interconnect length. The analysis provided by the tool has also allowed us to propose some new other key issues for interconnect power consumption optimization.

Based on the key issues some new power consumption optimization techniques are introduced (one of them called *Spatial Switching* is patented [1],[2]). The *Spatial Switching* technique which aims at removing the most energy consuming transitions (which are defined as the cross-transitions in our classification) show energetic power consumption gain that can rise up to 12% for a 5mm bus in the 65nm technology. These results include, of course, the extra power consumption due to the codecs; gains rise more with technological steps and bus length increasing.

Finally a possible extension of our work (tool and models) by the abstraction level elevation is proposed. First, our approach can be used to model *MESH* or *NoC* interconnects that are often used in *MPSoC* systems. Then, these results can be extended to be used in a *MDE* (*Model Driven Engineering*) approach in order to allow the power consumption estimations during the very first design phases of the system.

## References

[1] A. Courtay, J. Laurent, O. Sentieys, and N. Julien. Novel cross-transition elimination technique improving delay and power consumption for on-chip buses. *In the Proceedings of the IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, September 2008.

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