A Polynomial Based Approach to Wakeup Time and Energy Estimation in Power-Gated Logic Clusters

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Abstract *- Power gating has emerged as a promising technique for reduction of leakage current in sub-100nm CMOS circuits. To identify power gating opportunities within a system, logic circuits must be characterized for design overheads they present when power gating structures are inserted. In this paper, models are developed to quantify two mode transition overheads: wakeup time and wakeup energy using basic circuit parameters. First, a method to determine steady-state virtual-supply voltage in active mode is described and hence a model for virtual-supply voltage is presented based on certain heuristic approximations. Further, analytical expressions are derived for estimation of wakeup time and wakeup energy for a power-gated logic cluster using the proposed model. A key contribution of this paper is a study of nonlinear resistance based view of leakage current profiles of logic circuits. Finally, the application of proposed models to ISCAS85 benchmark circuits is demonstrated while also analyzing the accuracy of approximations used.*

Keywords **-** Leakage current, Power gating, Wakeup energy, Wakeup time

1 INTRODUCTION

An important consequence of MOSFET device scaling for constant field at sub-100nm dimensions is the steep increase in leakage current. Reduction in supply voltage necessitates a corresponding reduction in threshold voltage (V_{th}) to maintain gate overdrive resulting in an exponential increase in leakage current [1]. In ultra-low power applications that demand tight energy budgets, static power becomes a significant source of power consumption, possibly dominating dynamic power. Among the various techniques proposed to suppress leakage current, power gating has received significant attention and has emerged as a promising technique [2].

A power-gated circuit in its simplest form consists of a high-V_{th} *sleep transistor* connected in series with an ensemble of connected gates referred to as a logic cluster. A sleep transistor of PMOS type is connected between power supply rail (V_{dd}) and the power supply node, Virtual-Vdd (V_{Vdd}) of logic cluster whereas that of a NMOS type is connected between ground rail (Gnd) and ground node, Virtual-Gnd (V_{Gnd}) of logic cluster. The operation of sleep transistor is controlled by a signal connected to its gate. In this paper, a power-gated circuit refers to a cluster of logic gates with a PMOS transistor controlled by $SLEEP$ signal as shown in Fig. 1(a). Other forms of power-gated circuits are described in [2]. When $SLEEP$ is high, power supply to the logic is cutoff; V_{Vdd} decreases as the stored charge discharges. The circuit is then said to be in sleep mode. The leakage current decreases exponentially with V_{Vdd} resulting in energy savings. When $SLEEP$ is low, current flows through the sleep transistor to charge circuit capacitances. V_{Vdd} increases due to charging effect until it reaches a steady state value less than V_{dd}. A power-gated circuit is in steady state when there are no bounces on Virtual-Vdd due to short-circuit currents. We refer to this mode of operation as wakeup mode and the mode of operation after wakeup as active mode. The typical timing instants in a power gating cycle are shown in Fig. 2.

Power gating is an invasive technique and incurs a penalty in terms of area, supply/ground noise, delay and energy overhead for mode transitions [3]. Hence most works have viewed design of power-gated circuits as an optimization problem of partitioning logic into clusters [4] or designing a sleep transistor network [5] satisfying constraints of peak current, maximum delay degradation, minimum wakeup delay and minimum sleep transistor area [3]-[6]. Cell clustering algorithms have been proposed and wakeup schedules derived in [3] and [6] such that peak current and wakeup time constraints are satisfied. Fundamental to both iterative

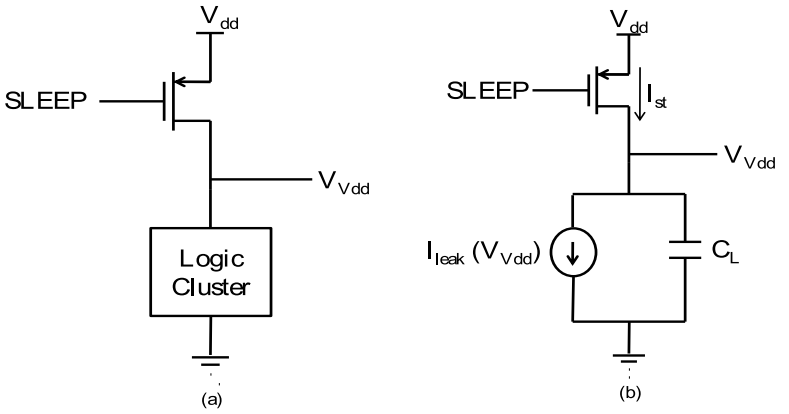

Figure 1. (a) Power-gated logic cluster of header type and (b) its equivalent circuit

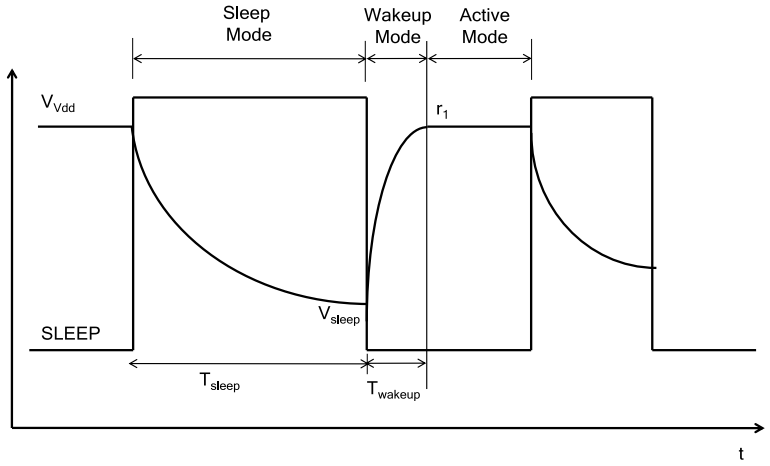

Figure 2. Typical timing instants in a power gating cycle

techniques is the estimation of wakeup time for each logic cluster. In [7] and [8], a need for wakeup latency estimation arises to quantify the effectiveness of proposed ground-bounce reducing techniques and intermediate strength power gating techniques respectively under a wakeup time constraint. In [9], Xu *et al.* have proposed numerical approaches based on linear regression for estimation of V_{Gnd} as a function of time in sleep mode. To estimate V_{Gnd} at $t = T_{sleep}$, a set of equations has to be solved region-by-region determined by sampling points on V_{Gnd} for $t < T_{sleep}$. In a scenario of logic clustering for run-time power gating, it may be necessary to evaluate V_{Gnd} repeatedly at different times for different cluster candidates. To extend the same method to wakeup mode, size dependent sleep transistor current characteristics needs to be incorporated. In this case an analytical model for V_{Gnd} would be highly desirable. This analysis is identically applicable to V_{Vdd} in a power-gated cluster with header type of sleep transistor used in this paper. Recent works have explored the

possibility of run-time leakage reduction where only parts of the overall circuit are put to sleep during short periods of inactivity [10][11]. The energy overhead and wakeup delay incurred during frequent mode transitions then become important parameters for consideration. In this context, a simple analytical model for estimation of wakeup time is useful when a need arises to estimate them for a number of cluster candidates iteratively during an optimization run.

In this paper, a method to estimate steady state Virtual-Vdd voltage of a power-gated logic cluster in sleep and wakeup modes from leakage current profiles of constituent logic gates and sleep transistor current is described. Further, using RC equivalent circuits for power-gated logic cluster, models are derived for Virtual-Vdd in sleep and wakeup modes based on initial and final conditions and circuit time constants obtained from heuristic approximations. Hence they are used to obtain closed form expressions for wakeup time and wakeup energy. In other words, key design constraints have been captured into a single model using three parameters: sleep transistor resistance in linear region, the leakage current profile and input capacitance of each cell. An important aspect of this approach is the compact representation of leakage current profiles of logic clusters using polynomials.

This paper is organized as follows. Section 2 describes the equivalent circuit of a power-gated combinational logic cluster. In Section 3, the analytical method leading to determination of wakeup time and wakeup energy is described. The sensitivity of wakeup time and energy to model parameters are derived. In Section 4 experimental results are presented and discussed. Section 5 concludes the paper.

2 Equivalent Circuit of a Power-Gated Logic Cluster

Models for subthreshold leakage current in short-channel MOSFET devices that capture its exponential behaviour with bias voltages have been described in detail in [12]. Using expressions for bias-dependent subthreshold current, compact models for leakage current have been developed at gate and circuit levels in a hierarchical way in [9]. It was shown that the leakage current can be represented by a voltage controlled current source (VCCS). Fig. 1(b) shows the equivalent circuit in terms of model parameters. The models were applied to logic gates in order to characterize them for leakage current at various voltages and input patterns. The total capacitance of the circuit was derived as sum of capacitances of all the inputs of all cells. We use the model at cell level in our work, but take a polynomial based approach to derive leakage current profile for the complete circuit [13]. For each cell, leakage current is determined at several voltages and the resulting profile is fitted with a polynomial

of degree N in V_{Vdd}. The leakage current profile for the complete circuit is then obtained as sum of profiles of all cells weighted by number of their occurrences in the circuit. Thus, for each type of cell S_i and input pattern j, the leakage current profile is represented by

$$I_{leak}(S_i, j) = \sum_{k=0}^{N} a_k(S_i, j) V_{Vdd}^k \tag{1}$$

where $a_k(S_i, j)$ denotes coefficients of the polynomial in V_{Vdd} for cell S_i and input pattern j. The total leakage current and the total load capacitance for $n(S_i, j)$ occurrences of each cell and each pattern are given by

$$I_{leak} = \sum_{i=0}^{P-1} \sum_{j=0}^{R_i-1} n(S_i, j) I_{leak}(S_i, j) \tag{2}$$

$$C_L = \sum_{i=0}^{P-1} n(S_i) \sum_{l=0}^{M_i-1} C_{il} \tag{3}$$

where P, R_i and M_i are number of types of cells, number of possible input combinations for cell S_i and fan-in of cell S_i respectively. For notational simplicity, total leakage current for the complete circuit is represented as

$$I_{leak} = \sum_{i=0}^{N} a_i V_{Vdd}^i \tag{4}$$

in the rest of the paper. It should be noted that (4) has the form of nonlinear resistance. The units of a_i's can be derived to be A/V^i. The physical meaning of a_i is not important to our problem.

In order to derive heuristics for equivalent resistance of the circuit it is useful to view (4) as follows. For each value of V_{Vdd}, the VCCS outputs a current given by (4). Therefore for each value of V_{Vdd} we infer that resistance of the circuit is given by

$$R_s(V_{Vdd}) = \frac{V_{Vdd}}{\sum_{i=0}^{N} a_i V_{Vdd}^i}. \tag{5}$$

In this paper we refer to R_s as *pseudo-resistance*. As leakage current decreases, R_s increases as in a circuit composed of cells with high-V_{th} transistors when compared with that of cells containing low-V_{th} transistors or a small circuit compared with a large circuit when composed of the same family of cells.

3 VIRTUAL-VDD MODEL

3.1 *Determination of Steady-State Virtual-Vdd Voltage*

Consider the equivalent circuit model in Fig. 1(b). Let the current through the sleep transistor during wakeup be denoted by I_{st}, the total leakage current through the VCCS by I_{leak} and the capacitive load charging current by I_{load}. Then,

$$I_{st}(t) = I_{leak} + I_{load}. \tag{6}$$

The current through the sleep transistor in linear region can be written as

$$I_{st}(t) = \frac{V_{dd} - V_{Vdd}(t)}{R_{lin}} \tag{7}$$

where R_{lin} denotes the resistance of sleep transistor in linear region. From (4), (7) and $I_{load} = C_L \frac{dV_{Vdd}}{dt}$, (6) becomes

$$\frac{dV_{Vdd}}{dt} = -\frac{1}{R_{lin}C_L}\left[(R_{lin}a_0 - V_{dd}) + (R_{lin}a_1 + 1)V_{Vdd} + R_{lin}\sum_{i=2}^{N} a_i V_{Vdd}^i\right]. \tag{8}$$

To determine solutions to (8), we first determine the equilibrium points, the values of $V_{Vdd}(t)$ at which the solution is constant, *i.e.*, $\frac{dV_{Vdd}}{dt} = 0$ as,

$$(R_{lin}a_0 - V_{dd}) + (R_{lin}a_1 + 1)V_{Vdd} + R_{lin}\sum_{i=2}^{N} a_i V_{Vdd}^i = 0. \tag{9}$$

Let $r_1, r_2, ..., r_N$ be the roots of Nth degree polynomial in (8). Then, (8) and (9) can be written in combined form as

$$\frac{dV_{Vdd}(t)}{dt} = -\frac{1}{R_{lin}C_L}\prod_{i=1}^{N}(V_{Vdd} - r_i) = 0. \tag{10}$$

All $V_{Vdd} = r_i$ constitute equilibrium points of (10). One of the roots r_i satisfying the interval of validity $V_{sleep} < r_i < V_{dd}$, where $V_{sleep} = V_{Vdd}(0)$ is determined to be the steady state Virtual-Vdd voltage.

3.2 *Wakeup Mode Virtual-Vdd Model*

During wakeup mode as V_{Vdd} increases towards V_{dd}, the operating point of the sleep transistor moves from saturation region to linear region. Let R_{wu} denote the effective resistance of the power-gated circuit when the operating point of sleep transistor is not in linear region. Further, in logic clusters where the wakeup dependency [3][4] is not satisfied due to changing logic states at some of the internal nodes in the cluster, short-circuit currents are generated. Therefore R_{wu} of power-gated circuit varies during wakeup mode. In general $R_{wu}(V_{Vdd}) = R_{st}(V_{Vdd})||R_s(V_{Vdd})$ where R_{st} is sleep transistor resistance. However for circuits with low

leakage current compared to I_{st}, $R_s(V_{Vdd})$ is high and hence $R_{wu}(V_{Vdd}) \approx R_{st}(V_{Vdd})$. In this paper, we choose a constant value $R_{wu}(V_{Vdd}) = R_{lin}$ heuristically in non-linear regions of operation so that a simplified treatment of V_{Vdd} is possible. In other words, the variation of $R_{wu}(V_{Vdd})$ from R_{lin} is neglected. The reasons for choice of this heuristic is explained further in subsection 3.4.

A model for Virtual-Vdd in wakeup mode is obtained as a solution of the ODE in (10). Among the possible solutions, the solution consistent with the initial and final conditions that $V_{Vdd} = V_{sleep}$ at $t = 0$ and $V_{Vdd} = 0.99V_{final}$ at $t = T_{wu}$ respectively is determined. We define wakeup time T_{wu} as the time required by Virtual-Vdd to attain 99% of its final value from the instant of wakeup transition of sleep transistor.

Let r_1 denote an equilibrium point of (10) such that $V_{sleep} < r_1 < V_{dd}$. The solution satisfying the intervals of validity and moving towards r_1 is determined as below:

$$\int \frac{dV_{Vdd}}{(V_{Vdd} - r_1)} = -\frac{1}{R_{wu}C_L} \int dt + K. \tag{11}$$

Applying the initial condition, (11) becomes,

$$V_{Vdd}(t) = r_1 + (V_{sleep} - r_1)e^{-\frac{t}{R_{wu}C_L}}. \tag{12}$$

Equation (12) gives a model for Virtual-V_{Vdd} in wakeup mode. Applying the final condition and replacing V_{final} by r_1, T_{wu} is given by,

$$T_{wu} = R_{wu}C_L \ln\left(\frac{r_1 - V_{sleep}}{0.01r_1}\right). \tag{13}$$

Wakeup energy is determined as

$$E_{wu} = \int_0^{T_{wu}} V_{dd}I_{st}(t)dt \tag{14}$$

or

$$E_{wu} = \frac{V_{dd}}{R_{wu}}\left[(V_{dd} - r_1)T_{wu} + R_{wu}C_L(V_{sleep} - r_1)(e^{\frac{-T_{wu}}{R_{wu}C_L}} - 1)\right]. \tag{15}$$

3.3 *Sleep Mode Virtual-Vdd Model*

In order to calculate T_{wu} and E_{wu} using (13) and (15) it is necessary to determine V_{sleep}. In other words, if the cluster is in sleep mode for a time interval T_{sleep}, $V_{sleep} = V_{Vdd}(T_{sleep})$. It should be noted that for simplicity both mode transitions are assumed to occur at $t = 0$, so that the initial condition for sleep mode is $V_{Vdd}(0) = r_1$. In sleep mode, the sleep transistor

is cut-off so that a leakage current $I_{st,leak}$ flows through it. I_{load} in (5) is now a discharging current. Hence (5) for sleep mode can be written as,

$$-C_L\frac{dV_{Vdd}}{dt} = -(a_0 - I_{st,leak}) - \sum_{i=1}^{N} a_i V_{Vdd}^i. \tag{16}$$

Rewriting (16) similar to (8),

$$\frac{dV_{Vdd}}{dt} = -\frac{1}{R_s C_L}\left[-R_s(a_0 - I_{st,leak}) - R_s\sum_{i=1}^{N} a_i V_{Vdd}^i\right]. \tag{17}$$

Equation (17) does not have solutions in closed form. To develop an approximation we consider a heuristic for choice of R_s as explained in the subsection 3.5. Denoting R_{sp} as the pseudo-resistance chosen by applying the heuristic and writing equations analogous to (8) and (10), the model for Virtual-Vdd in sleep mode can be derived as below:

$$\frac{dV_{Vdd}}{dt} = -\frac{1}{R_{sp} C_L}\left[-R_{sp}(a_0 - I_{st,leak}) - R_{sp}\sum_{i=1}^{N} a_i V_{Vdd}^i\right] \tag{18}$$

$$\frac{dV_{Vdd}}{dt} = -\frac{1}{R_{sp} C_L}\prod_{i=1}^{N}(V_{Vdd} - r_i^s) = 0 \tag{19}$$

where r_i^s represents roots of the polynomial in sleep context. Let r_1^s denote an equilibrium point of (19) such that $r_1 < r_1^s < 0$. Then,

$$V_{Vdd}(t) = r_1^s + e^{-\frac{t}{R_{sp}C_L} + K^s}. \tag{20}$$

At the end of active mode, the value of Virtual-Vdd satisfies $r_1 - \Delta V_{Vdd,max} \leq V_{Vdd} \leq r_1$ where $\Delta V_{Vdd,max}$ is the maximum degradation of V_{Vdd} due to dynamically changing inputs of logic cluster. In this work, it is assumed that the power-gated logic cluster remains in active mode for a duration long enough with appropriate input conditions that $V_{Vdd} = r_1$ at the end of active mode. This assumption is mostly true in low-power, low-performance circuits. Hence, applying the initial condition that $V_{Vdd}(t) = r_1$ at $t = 0$ and final condition that $V_{Vdd} = V_{sleep}$ at $t = T_{sleep}$ we have

$$V_{Vdd}(t) = r_1^s + (r_1 - r_1^s)e^{-\frac{t}{R_{sp}C_L}} \tag{21}$$

$$V_{sleep} = r_1^s + (r_1 - r_1^s)e^{-\frac{T_{sleep}}{R_{sp}C_L}}. \tag{22}$$

We note that (12) and (21) are similar except for circuit parameters in form of time constants and terminal conditions.

3.4 *Heuristic for* R_{wu}

The I_{SD} vs V_{SD} characteristics of a PMOS transistor from an industrial 65nm CMOS technology library and its linear approximation for $V_{SD} \leq V_{DSAT}$ are shown in Fig. 3. It can be seen that for $V_{SD} \leq 0.227V$, the characteristics can be approximated by the linear model in (7), with R_{lin} being the resistance of sleep transistor in linear region determined as the inverse of slope of I_{SD} vs V_{SD} characteristics. Table I shows the drain current characteristics of PMOS transistor for different widths and corresponding resistances in linear region. It has been observed from experiments that the time taken for Virtual-Vdd to reach $0.99r_1$ from 0.773V (or $V_{SD} = 0.227V$) is about 54% of the wakeup time. Therefore R_{lin} determines evolution of V_{Vdd} for a significantly higher time than any other value for $R_{wu}(V_{Vdd})$ in other regions of operation in wakeup mode. Hence as a heuristic, we choose R_{lin} for effective resistance R_{wu}.

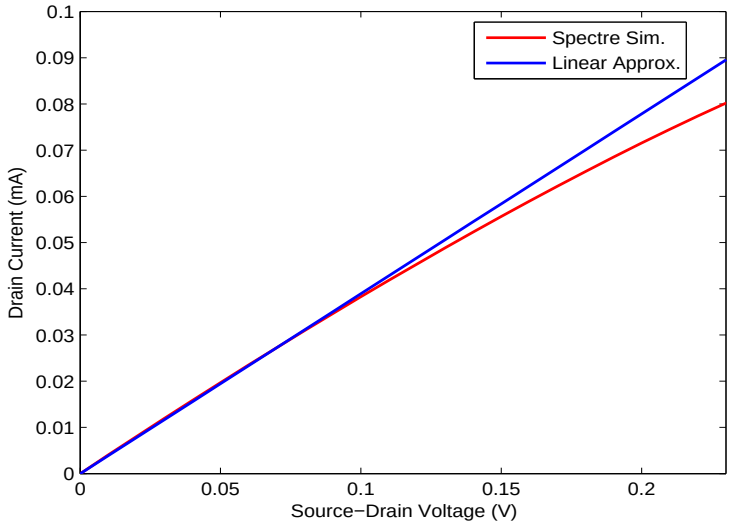

Figure 3. I_{SD} vs V_{SD} characteristics of PMOS transistor in linear region $[0 \leq V_{SD} \leq V_{DSAT}](W = 0.54\mu m, L = 0.06\mu m)$

3.5 *Heuristic for* R_s

The voltage dependent pseudo-resistance changes as V_{Vdd} evolves with time according to (21). Hence it can be inferred that the time constant R_sC_L also varies with time. In our experiments, we have observed that in large logic clusters, the values of pseudo-resistance and its dynamic range are less than that for small logic clusters as leakage currents are higher in the former case. A typical variation of pseudo-resistance with V_{Vdd} is shown in Fig. 4 in

TABLE I

I_{SD} **VS** V_{SD} **CHARACTERISTICS OF 65NM PMOS TRANSISTOR (**$L = 0.06\mu m$**) IN LINEAR REGION AT 100°C AND** $V_{SG} = 1V$

W (μm)	$I_{SD}(\mu A)$ (V_{SD} = 0.05V)	$I_{SD}(\mu A)$ (V_{SD} = 0.227V)	R_{lin} (kΩ)
0.54	19.56	88.43	2.57
1.2	42.01	189.14	1.203
2.4	82.72	371.93	0.612
4.8	156.95	706.64	0.322
9.6	303.12	1363.0	0.167
12	376.25	1697.71	0.134

the next section. The effect of a larger value of pseudo-resistance on V_{Vdd} is that it takes a longer time for V_{Vdd} to change between specific voltage levels than with smaller values. Typically, higher values of pseudo-resistance determine V_{Vdd} after about 4 time constants of sleep time. Considering these observations, we choose R_{sp} as the pseudo-resistance at $V_{Vdd} = r_1$ for R_s.

3.6 *Sensitivity of* T_{wu} *and* E_{wu} *on* V_{sleep}, R_{wu} *and* C_L

Heuristic approximation of R_s can impact V_{sleep}, a parameter which wakeup time and wakeup energy depend on. Hence sensitivity factors are derived to evaluate the impact of variations in V_{sleep} on T_{wu} and E_{wu}. Let $S_t^{(1)}$ and $S_e^{(1)}$ denote sensitivities of wakeup time and wakeup energy to V_{sleep} respectively. By definition, $S_t^{(1)} = \frac{\partial T_{wu}}{\partial V_{sleep}}$ and $S_e^{(1)} = \frac{\partial E_{wu}}{\partial V_{sleep}}$. From (13) and (15), the expressions for sensitivity factors are derived as,

$$S_t^{(1)} = \frac{-R_{wu}C_L}{r_1 - V_{sleep}}, \qquad S_e^{(1)} = \frac{V_{dd}(V_{dd} - V_{sleep})C_L}{r_1 - V_{sleep}}. \tag{23}$$

The bounds on variation of T_{wu} and E_{wu} with variation of V_{sleep} are thus obtained from

$$\begin{aligned}(\Delta T_{wu})_{max} &= |S_t^{(1)}|(\Delta V_{sleep})_{max} \\ (\Delta E_{wu})_{max} &= S_e^{(1)}(\Delta V_{sleep})_{max}.\end{aligned} \tag{24}$$

Similarly the other pairs of sensitivity factors *w.r.t* R_{wu} and C_L are given by

$$S_t^{(2)} = \frac{\partial T_{wu}}{\partial R_{wu}} = C_L \ln\left(\frac{r_1 - V_{sleep}}{0.01 r_1}\right) \qquad S_e^{(2)} = \frac{\partial E_{wu}}{\partial R_{wu}} = 0 \tag{25}$$

and

$$S_t^{(3)} = \frac{\partial T_{wu}}{\partial C_L} = R_{wu} \ln\left(\frac{r_1 - V_{sleep}}{0.01 r_1}\right)$$

$$S_e^{(3)} = \frac{\partial E_{wu}}{\partial C_L} = V_{dd}\left[(V_{dd} - r_1)\ln\left(\frac{r_1 - V_{sleep}}{0.01 r_1}\right) + (0.99 r_1 - V_{sleep})\right]. \quad (26)$$

The term r_1 is considered to be a constant as it depends on V_{dd}, a_i and R_{lin}, which can be determined with high accuracy. In the next section, these equations are examined in the context of our experiments to analyze variations of wakeup time and energy *w.r.t* variations in model parameters. It should be noted that impact of short-circuit currents at wakeup on T_{wu} and E_{wu} have been neglected in this work. They create the effect of altering R_{wu} during wakeup. A model to estimate short-circuit currents in logic gates with varying virtual supply voltage would be required to account for its effects. It is proposed to take it up as future work.

4 Experimental Results

To validate the model and approximations proposed above we compare its application to eight ISCAS85 benchmark circuits [14] listed in Table II with simulations using Spectre circuit simulator of Cadence Virtuoso ICFB. These circuits represent a maximum variation of about 9× in gate complexity and equivalent circuit capacitance between each other. The circuits are synthesized with a restricted set of logic gates as enumerated in Table II. For half of the circuits mentioned in the table, the cell library has two additional cells of half adder and full adder.

TABLE II

FEATURES OF ISCAS BENCHMARK CIRCUITS

Circuit	c7552	c6288	c5315	c3540	c2670	c1908	c499	c432
# of NAND Gate Equivalents	1563	1504	1402	1022	642	304	354	182
C_L(pF)	2.892	3.171	2.559	1.955	1.148	0.606	0.601	0.351
Cells used for Synthesis	NAND2, NOR2, XOR2, AND2, INV - c7552, c5315, c3540, c2670 + Half Adder (HA), Full Adder (FA) - c6288, c1908, c499, c432							

Each standard cell in Table II is characterized for leakage current for a supply voltage variation between 0 and 1V for all input patterns at an operating temperature of 100°C using Spectre. The standard cells are chosen from an industrial 65nm CMOS technology library. Each of these profiles are then fitted with polynomials using MATLAB. The degree of the polynomials are chosen such that the modeled leakage current is within 0.1% of the corresponding value obtained from Spectre simulation. Hence, a leakage current profile is

determined for the circuit by weighting the polynomials with number of occurrences in the gate netlist and adding them together to form I_{leak} in (4). A leakage current profile for the circuit is shown in Fig. 4. From this curve, pseudo-resistance is determined at each point in the Virtual-Vdd segment. Fig. 4 shows such a variation for c6288.

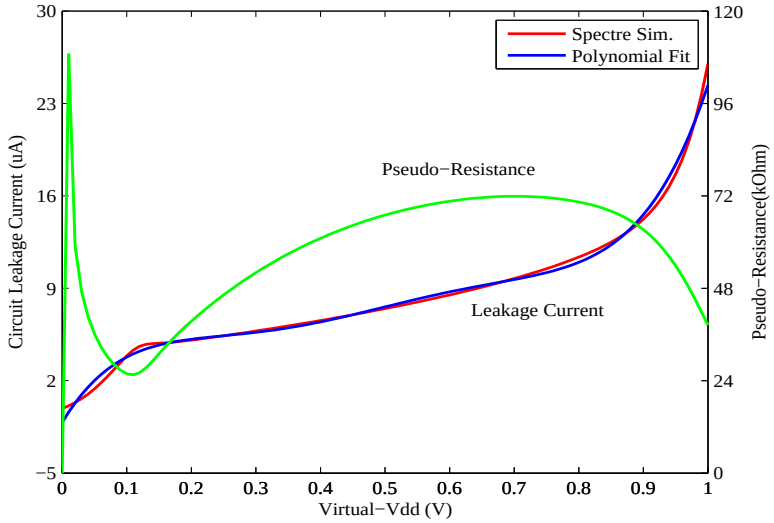

Figure 4. Variation of Circuit Leakage Current and Pseudo-Resistance with Virtual-Vdd in c6288 ($N = 7$)

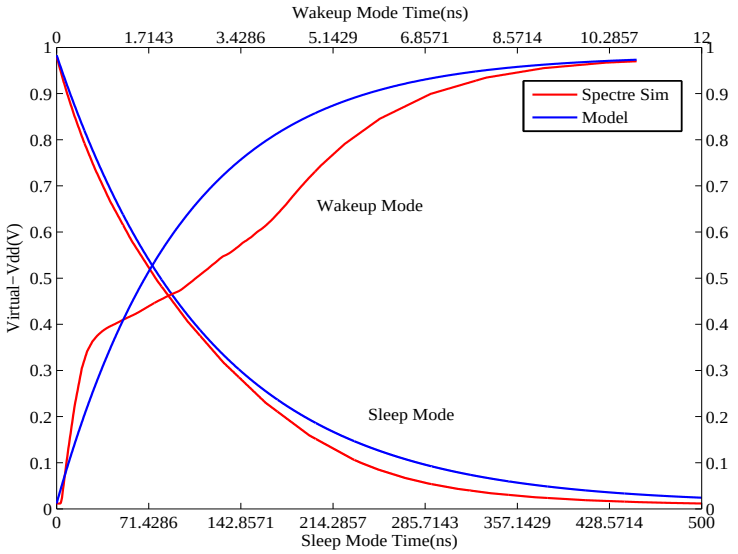

Figure 5. Virtual-Vdd in Wakeup and Sleep Modes ($W = 1.2\mu m$) in c3540

For our simulations with Spectre, the supply voltage V_{dd} is set to 1.0V. The evolution of Virtual-Vdd during wakeup and sleep modes is shown in Fig. 5. In Table III, the maximum

voltage levels attained by Virtual-Vdd with sleep transistors of different sizes for c6288, c5315 and c432 are given. Using the method described in section 3.1, they are determined to be within an error margin of 1.9%. Table IV shows results from Spectre simulations and application of (13) to determine wakeup time for different sleep transistor widths for three circuits. It should be noted that the transistor widths considered are not designed to meet a particular peak current constraint [3] as we do not address the problem of logic clustering in this work. Accuracy of wakeup times are affected by accuracy of both R_{wu} and C_L as indicated by sensitivity equations in subsection 3.6. Additional model parameters may be needed to account for R_{wu} variations in saturation region of sleep transistor operation to reduce relative errors and is proposed to be taken up for future work. Further, Table V provides a comparison of estimated wakeup energy with Spectre simulations. In general the values do not show significant variations across R_{lin} (different W) as expected from expression for $S_e^{(2)}$. Table VI shows average errors in estimation of the three quantities across different transistor sizes for eight ISCAS85 benchmark circuits considered in this work. On an average wakeup times and wakeup energies have been estimated within an error margin of 21.1% and 17.1% respectively.

TABLE III

MAXIMUM VIRTUAL-VDD AFTER WAKEUP

W (μm)	r_1 (mV) Eq.(10)			Max. V_{Vdd} (mV) Spectre			Relative Error (%)		
	c6288	c5315	c432	c6288	c5315	c432	c6288	c5315	c432
0.54	959.9	953.4	990.5	948.0	938.7	991.7	1.3	1.6	0.1
1.2	978.5	974.7	995.3	974.2	969.4	996.1	0.4	0.5	0.1
2.4	988.2	985.9	997.5	986.5	983.9	998.0	0.2	0.2	0.1
4.8	993.5	992.2	998.7	992.8	991.4	998.9	0.1	0.1	0.0
9.6	996.5	995.8	999.3	996.2	995.5	999.4	0.0	0.0	0.0
12	997.0	996.2	999.5	997.0	996.4	999.5	0.0	0.0	0.0

5 CONCLUSION

In this paper, we have presented a model for Virtual-Vdd voltage from which wakeup time and wakeup energy of a power-gated logic cluster can be estimated. Polynomial representations were used for static current profiles leading to development of the model. In active mode, steady state Virtual-Vdd can be used to determine leakage energy of the cluster. In sleep

TABLE IV

WAKEUP TIME COMPUTATIONS IN C6288, C5315 AND C432

W (μm)	Wakeup Time (ns) Spectre			Wakeup Time (ns) Eq. (13)			Relative Error (%)		
	c6288	c5315	c432	c6288	c5315	c432	c6288	c5315	c432
0.54	46.74	30.04	3.89	37.23	30.22	4.13	20.3	0.6	6.2
1.2	22.24	14.44	1.89	17.42	14.14	1.93	21.6	2.0	2.5
2.4	12.04	7.57	0.924	8.86	7.20	1.25	26.3	4.9	36.0
4.8	6.52	4.12	0.588	4.66	3.79	0.52	28.4	8.0	10.3
9.6	3.62	2.83	0.384	2.424	1.97	0.27	33.0	30.4	27.4
12	3.03	1.83	0.335	1.955	1.58	0.22	35.5	13.2	32.9

TABLE V

WAKEUP ENERGY COMPUTATIONS IN C6288, C5315 AND C432

W (μm)	Wakeup Energy (pJ) Spectre			Wakeup Energy (pJ) Eq. (15)			Relative Error (%)		
	c6288	c5315	c432	c6288	c5315	c432	c6288	c5315	c432
0.54	3.871	2.471	0.259	3.48	2.938	0.348	10.0	18.9	34.6
1.2	3.721	2.338	0.258	3.27	2.742	0.342	12.1	17.3	32.4
2.4	3.607	2.286	0.261	3.16	2.640	0.343	12.3	15.5	31.3
4.8	3.598	1.936	0.266	3.10	2.585	0.337	13.7	33.5	26.7
9.6	3.669	2.292	0.273	3.07	2.555	0.335	16.2	11.6	22.6
12	3.705	2.304	0.275	3.07	2.552	0.334	17.1	10.8	21.4

mode, the model can be used to estimate leakage energy savings in inactive states of the cluster due to power gating. In other words, key parameters used as optimization criteria for logic clustering have been captured in simple closed form expressions.

Our simulations and application of the model to eight ISCAS85 benchmark circuits with an industrial 65nm CMOS technology library show that on an average wakeup time and wakeup energy can be estimated within an error margin of 21.1% and 17.1% over 22$\times$ variation in transistor sizes. The steady-state Virtual-Vdd is shown to be determined within 1.9% of error. Coupled with sensitivity factors, error bounds can be determined for wakeup time to make design trade-offs for logic clustering. In future we propose to improve the model by introducing additional parameters to address wakeup time estimation errors and use this model to determine energy savings in presence of wakeup overheads.

TABLE VI

AVERAGE RELATIVE ERRORS IN ESTIMATION OF MAXIMUM V_{Vdd}, WAKEUP TIME AND WAKEUP ENERGY IN ISCAS BENCHMARK CIRCUITS

Circuit	Max. V_{Vdd} (%)	T_{wu} (%)	E_{wu} (%)
c7552	0.2	17.9	2.9
c6288	0.3	27.5	13.6
c5315	0.4	9.8	17.9
c3540	0.3	8.4	32.6
c2670	0.2	17.0	7.3
c1908	0.2	33.6	15.7
c499	0.1	35.2	18.9
c432	0.1	19.2	28.2
Average	0.2	21.1	17.1

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