Wakeup Time and Wakeup Energy Estimation in Power-Gated Logic Clusters

Vivek T D, Olivier Sentieys
IRISA Laboratory, ENSSAT
University of Rennes 1, Lannion, France
{*vivektd,sentieys*}*@irisa.fr*

Steven Derrien
IRISA Laboratory, IFSIC
University of Rennes 1, Rennes, France
sderrien@irisa.fr

***Abstract*—Run-time power gating for aggressive leakage reduction has brought into focus the cost of mode transition overheads due to frequent switching between sleep and active modes of circuit operation. In order to design circuits for effective power gating, logic circuits must be characterized for overheads they present during mode transitions. In this paper, we describe a method to determine steady-state virtual-supply voltage in active mode and hence present a model for virtual-supply voltage in terms of basic circuit parameters. Further, we derive expressions for estimation of two mode transition overheads: wakeup time and wakeup energy for a power-gated logic cluster using the proposed model. Finally we demonstrate its application to four ISCAS benchmark circuits while also analyzing the accuracy of approximations used in the model.**

***Keywords*-Leakage current, power gating, wakeup time**

I. Introduction

As MOSFET devices scale down to sub-100nm dimensions, static power becomes a significant source of power consumption, especially in ultra-low power applications, due to increase in leakage current. Reducing threshold voltage (V_{th}) to maintain gate overdrive for adequate performance has resulted in an exponential increase in subthreshold leakage current [1]. Among the various techniques proposed to suppress leakage current, power gating has received significant attention and has emerged as a promising technique [2].

A power-gated circuit in its simplest form consists of a high-V_{th} PMOS or NMOS *sleep* transistor connected between power supply rail (V_{dd}) and the power supply node Virtual-V_{dd} (V_{Vdd}) of logic cluster or between ground rail (Gnd) and ground node Virtual-Gnd (V_{Gnd}) of logic cluster respectively. The gate of the sleep transistor is connected to a control signal to switch the transistor between ON and OFF states. In our work, a power-gated circuit refers to a cluster of logic gates with a PMOS transistor controlled by $SLEEP$ signal as shown in Fig. 1(a). Other forms of power-gated circuits are described in [2]. When $SLEEP$ is high, power supply to the logic is cutoff; V_{Vdd} decreases as the stored charge discharges. The circuit is said to be in sleep mode. The leakage current decreases exponentially with V_{Vdd} resulting in energy savings. When $SLEEP$ is low, current flows through the sleep transistor to charge circuit capacitances. V_{Vdd} increases due to charging effect

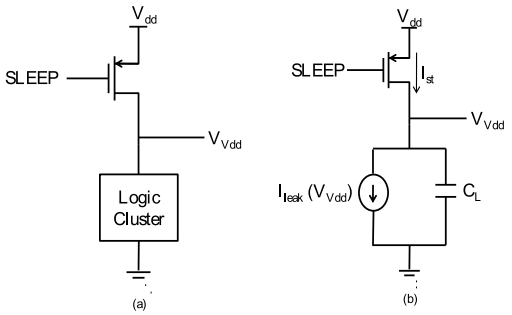

Figure 1. (a) Power-gated logic cluster of header type and (b) its equivalent circuit

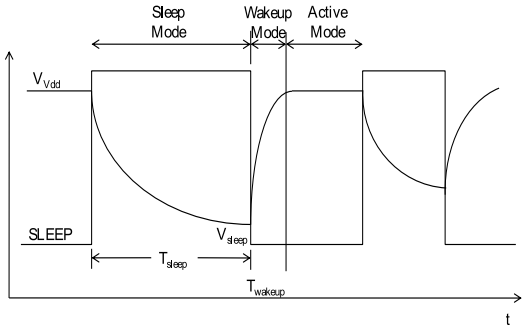

Figure 2. Typical timing instants in a power gating cycle

until it reaches a steady state value less than V_{dd}. A power-gated circuit is in steady state when there are no bounces on Virtual-V_{dd} due to short-circuit currents. For clarity in presentation, we refer to this mode of operation as wakeup mode and the mode of operation after wakeup as active mode. The typical timing instants in a power gating cycle are shown in Fig. 2. Power gating is an invasive technique and incurs a penalty in terms of area, supply-ground noise, delay and energy overhead for mode transitions [3].

In this paper, we describe a method to estimate Virtual-V_{dd} voltage after wakeup using leakage current profiles of constituent logic gates. Further, models are derived for Virtual-V_{dd} in sleep and wakeup modes based on circuit time constants, and hence used to obtain expressions for wakeup time and wakeup energy of a power-gated logic cluster. In other words, key parameters indicative of design constraints

1063-9667/11 $26.00 © 2011 IEEE
DOI 10.1109/VLSID.2011.18

have been captured into a single model.

This paper is organized as follows. Section II gives an overview of related work. Section III describes the model of a power-gated combinational logic cluster. In Section IV, the analytical method leading to determination of wakeup time and wakeup energy is described. Section V shows experimental results. Section VI concludes the paper.

II. Related Work

Most works have viewed design of power-gated circuits as an optimization problem of partitioning logic into clusters or designing a sleep transistor network satisfying constraints of peak current, maximum delay degradation, minimum wakeup delay and minimum sleep transistor area [3][4][5][6]. Recent works have explored the possibility of run-time leakage reduction where only parts of the overall circuit are put to sleep during short periods of inactivity [7][8]. In this context, energy overhead and wakeup delay incurred during frequent mode transitions become important parameters for consideration in design of power-gated circuits. In [9], wakeup time and wakeup energy have been shown to depend on steady-state Virtual-Gnd voltage linearly and quadratically respectively. In [10], Xu *et al.,* have proposed numerical approaches based on linear regression for estimation of V_{Gnd} as a function of time. In a scenario of logic clustering for run-time power gating, it may be necessary to evaluate V_{Gnd} repeatedly at different times for different cluster candidates. A limitation of their approach is that, to estimate V_{Gnd} at $t = T_{sleep}$, a set of equations have to be solved region-by-region determined by sampling points on V_{Gnd} for $t < T_{sleep}$. Further, selection of sampling points for lesser number of regions requires unequal spacing between successive points, which is not trivial to determine for different cluster candidates. In this work, we present a model for Virtual-V_{dd} based on initial and final conditions, and circuit time constants obtained from heuristic approximations. Hence closed form expressions are derived for V_{Vdd} in both wakeup and sleep modes and are used to estimate wakeup time and wakeup energy.

III. Power-Gated Logic Cluster Model

Models for subthreshold leakage current that capture its exponential behaviour with voltage have been derived at device, gate and circuit levels in [10]. Fig. 1(b) shows the equivalent circuit in terms of model parameters. It was shown that the leakage current can be represented by a voltage controlled current source (VCCS). The models were applied to logic gates in order to characterize them for leakage current at various voltages and input patterns. The total capacitance of the circuit was derived as sum of capacitances of all the inputs of all cells. We use the model in our work, but take a polynomial based approach to derive leakage current profile for the complete circuit. For each cell, leakage current is determined at several voltages and the resulting profile is fitted with a polynomial of degree N in V_{Vdd}. The leakage current profile for the complete circuit is then obtained as sum of profiles of all cells weighted by number of their occurrences in the circuit. Thus, for each type of cell S_i and input pattern j, the leakage current profile is represented by

$$I_{leak}(S_i, j) = \sum_{k=0}^{N} a_k(S_i, j) V_{Vdd}^k \tag{1}$$

where $a_k(S_i, j)$ denotes coefficients of the polynomial in V_{Vdd} for cell S_i and input pattern j. The total leakage current and the total load capacitance for $n(S_i, j)$ occurrences of each cell and each pattern are given by

$$I_{leak} = \sum_{i=0}^{P-1} \sum_{j=0}^{R_i-1} n(S_i, j) I_{leak}(S_i, j) \tag{2}$$

$$C_L = \sum_{i=0}^{P-1} n(S_i) \sum_{l=0}^{M_i-1} C_{il} \tag{3}$$

where P, R_i and M_i are number of types of cells, number of possible input combinations for cell S_i and fan-in of cell S_i respectively. For notational simplicity, total leakage current for the complete circuit is represented as

$$I_{leak} = \sum_{i=0}^{N} a_i V_{Vdd}^i \tag{4}$$

in the rest of the paper.

IV. Virtual-Vdd Model

A. Determination of Steady-State Virtual-V_{dd} Voltage

Consider the equivalent circuit model in Fig. 1(b). Let the current through the sleep transistor during wakeup be denoted by I_{st}, the total leakage current through the VCCS by I_{leak} and the capacitive load charging current by I_{load}. Then,

$$I_{st}(t) = I_{leak} + I_{load} \tag{5}$$

The current through the sleep transistor can be written as [5]

$$I_{st}(t) = \frac{(V_{dd} - V_{Vdd}(t))}{R_{wu}} \tag{6}$$

where R_{wu} denotes the effective resistance. During wakeup mode as V_{Vdd} increases towards V_{dd}, the logic states at the inputs of some of the gates in the cluster change resulting in short circuit currents. This effect has been described as due to *wakeup dependency* not being met by the logic cluster and has been addressed as part of logic clustering problem in [3], [4]. Hence the current through sleep transistor varies during wakeup mode. Therefore, it may be inferred that effective resistance R_{wu} also varies with time during wakeup. However, in this paper we derive a heuristic leading to a constant

R_{wu} so that simplified treatment of V_{Vdd} is possible. From (4), (6) and with $I_{load} = C_L \frac{dV_{Vdd}(t)}{dt}$ (5) becomes,

$$\frac{dV_{Vdd}(t)}{dt} = -\frac{1}{R_{wu}C_L}[(R_{wu}a_0 - V_{dd}) + (R_{wu}a_1 + 1)V_{Vdd}(t) + R_{wu}\sum_{i=2}^{N} a_i V_{Vdd}^i(t)] \quad (7)$$

To determine solutions to (7), we first determine the equilibrium points, the values of $V_{Vdd}(t)$ at which the solution is constant, *i.e.,* $\frac{dV_{Vdd}(t)}{dt} = 0$ as,

$$(R_{wu}a_0 - V_{dd}) + (R_{wu}a_1 + 1)V_{Vdd}(t) + R_{wu}\sum_{i=2}^{N} a_i V_{Vdd}^i(t) = 0 \quad (8)$$

Hence among the possible solutions, the solution consistent with the initial and final conditions that $V_{Vdd} = V_{sleep}$ at $t = 0$ and $V_{Vdd} = 0.99(\alpha V_{dd})$ at $t = T_{wu}$ respectively is determined. Here, V_{sleep} is the final value attained by Virtual-V_{dd} just before wakeup transition. We define wakeup time T_{wu} as the time required by Virtual-V_{dd} to attain 99% of its final value from the instant of wakeup transition of sleep transistor. The final value of V_{Vdd} is expressed in terms of V_{dd} to denote an IR drop [4] across the sleep transistor. It is quantified by $\alpha < 1$.

Let $r_1, r_2, ...r_N$ be the roots of N-th degree polynomial in (7). Then, (7) and (8) can be written as

$$\frac{dV_{Vdd}(t)}{dt} = -\frac{1}{R_{wu}C_L}\prod_{i=1}^{N}(V_{Vdd} - r_i) = 0 \quad (9)$$

All $V_{Vdd} = r_i$ constitute the equilibrium points of (9). One of the roots r_i satisfying the interval of validity $V_{sleep} < r_i < V_{dd}$, is determined to be the steady state Virtual-V_{dd} voltage.

B. Wakeup Mode V_{Vdd} Model

Let r_1 denote an equilibrium point of (9). The solution satisfying the intervals of validity and moving towards r_1 is determined as below:

$$\int \frac{dV_{Vdd}}{(V_{Vdd} - r_1)} = -\frac{1}{R_{wu}C_L}\int dt + K \quad (10)$$

or

$$V_{Vdd}(t) = r_1 + e^{-\frac{t}{R_{wu}C_L} + K} \quad (11)$$

Applying the initial condition, (11) becomes,

$$V_{Vdd}(t) = r_1 + (V_{sleep} - r_1)e^{-\frac{t}{R_{wu}C_L}} \quad (12)$$

(12) gives a model for estimation of Virtual-V_{Vdd} in wakeup mode. Applying the final condition and replacing αV_{dd} by r_1, T_{wu} is given by,

$$T_{wu} = R_{wu}C_L \ln\left(\frac{r_1 - V_{sleep}}{0.01 r_1}\right) \quad (13)$$

Wakeup energy is determined as

$$E_{wu} = \int_0^{T_{wu}} V_{dd} I_{st}(t) dt \quad (14)$$

or

$$E_{wu} = \frac{V_{dd}}{R_{wu}}[(V_{dd} - r_1)T_{wu} + R_{wu}C_L(V_{sleep} - r_1)(e^{\frac{-T_{wu}}{R_{wu}C_L}} - 1)] \quad (15)$$

C. Sleep Mode V_{Vdd} Model

In order to calculate T_{wu} and E_{wu} using (13) and (15) it is necessary to determine V_{sleep}. In other words, if the cluster is in sleep state for a time interval T_{sleep}, $V_{sleep} = V_{Vdd}(T_{sleep})$. It should be noted that for simplicity both mode transitions are assumed to occur at $t = 0$, so that the initial condition for sleep mode is $V_{Vdd}(0) = r_1$. In sleep mode, the sleep transistor is cut-off so that only a leakage current $I_{st,leak}$ flows through it. I_{load} in (5) is now a discharging current. Hence (5) for sleep mode can be written as,

$$-C_L\frac{dV_{Vdd}(t)}{dt} = -(a_0 - I_{st,leak}) - \sum_{i=1}^{N} a_i V_{Vdd}^i(t) \quad (16)$$

For each value of V_{Vdd}, the VCCS outputs a current $I_{V_{Vdd}}$. Therefore it may be assumed that for each value of V_{Vdd}, a quantity $R_s(V_{Vdd}) = \frac{V_{Vdd}}{I_{V_{Vdd}}}$ with units of resistance exists. In this paper we call it *pseudo-resistance*. Rewriting (16) similar to (7),

$$\frac{dV_{Vdd}(t)}{dt} = -\frac{1}{R_s C_L}[-R_s(a_0 - I_{st,leak}) - R_s\sum_{i=1}^{N} a_i V_{Vdd}^i(t)] \quad (17)$$

(17) does not have solutions in closed form [10]. To develop an approximation we consider a heuristic for choice of R_s as explained in the subsection IV-E. Denoting R_{sp} as the pseudo-resistance chosen by applying the heuristic and writing equations analogous to (7) and (9), the model for Virtual-V_{dd} in sleep mode can be derived as below:

$$\frac{dV_{Vdd}(t)}{dt} = -\frac{1}{R_{sp}C_L}[-R_{sp}(a_0 - I_{st,leak}) - R_{sp}\sum_{i=1}^{N} a_i V_{Vdd}^i(t)] \quad (18)$$

$$\frac{dV_{Vdd}(t)}{dt} = -\frac{1}{R_{sp}C_L}\prod_{i=1}^{N}(V_{Vdd} - r_i^s) = 0 \quad (19)$$

where r_i^s represents roots of the polynomial in sleep context.

$$V_{Vdd}(t) = r_1^s + e^{-\frac{t}{R_{sp}C_L} + K^s} \quad (20)$$

Applying the initial condition that $V_{Vdd}(t) = r_1$ at $t = 0$ and final condition that $V_{Vdd} = V_{sleep}$ at $t = T_{sleep}$ we have

$$V_{Vdd}(t) = r_1^s + (r_1 - r_1^s)e^{-\frac{t}{R_{sp}C_L}} \quad (21)$$

W (μm)	$I_{SD}(\mu A)$ (V_{SD} = 0.05V)	$I_{SD}(\mu A)$ (V_{SD} = 0.3V)	R_{lin} (kΩ)
0.54	19.56	96.80	3.237
1.2	42.01	205.60	1.528
2.4	82.72	404.40	0.777
4.8	156.95	775.29	0.404
9.6	303.12	1501.33	0.208
12	376.25	1867.30	0.167

Table I
I_{SD} VS V_{SD} CHARACTERISTICS OF PMOS TRANSISTOR IN LINEAR REGION (AT 100°C, V_{SG}=1V)

$$V_{sleep} = r_1^s + (r_1 - r_1^s)e^{-\frac{T_{sleep}}{R_{sp}C_L}} \tag{22}$$

We note that (12) and (21) are similar except for circuit parameters in form of time constants and terminal conditions.

D. Heuristic for R_{wu}

The I_{SD} vs V_{SD} characteristics of a PMOS transistor from an industrial 65nm CMOS technology library and its linear approximation for $V_{SD} \leq (V_{SG} - |V_{th}|)$ is shown in Fig. 3. It can be seen that for $V_{SD} \leq 0.3V$, the characteristics can be approximated well with a linear model similar to (6) with $R_{wu} = R_{lin}$, the resistance of sleep transistor in linear region determined as the inverse of slope of I_{SD} vs V_{SD} characteristics. Table I shows the drain current characteristics of PMOS transistor for different widths and corresponding resistances in linear region. It can be shown from (12) and (13) that the time taken for Virtual-V_{dd} to reach $0.99r_1$ from 0.7V (or $V_{SD} = 0.3V$) is about 75% of the wakeup time and therefore this resistance determines the time constant for most of the time in wakeup mode. As a heuristic, we choose R_{lin} for effective resistance R_{wu}.

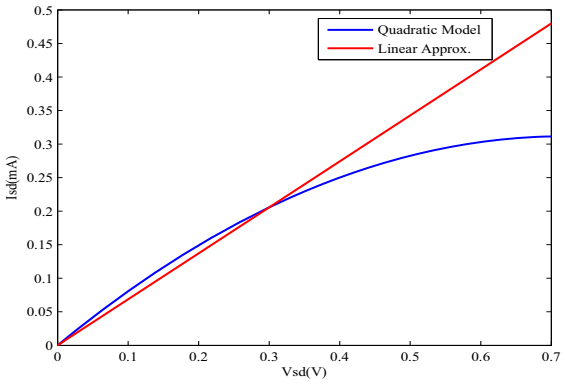

Figure 3. I_{SD} vs V_{SD} characteristics of PMOS transistor (W=1.2μm)

E. Heuristic for R_s

The voltage dependent pseudo-resistance changes as V_{Vdd} evolves with time according to (21). Hence it can be inferred that the time constant R_sC_L also varies with time. In our experiments, we have observed that in large logic clusters, the values of pseudo-resistance and its dynamic range are less than that for small logic clusters as leakage currents are higher in the former case. A typical variation of pseudo-resistance with V_{Vdd} is shown in Fig. 4 in the next section. The effect of a larger value of pseudo-resistance on V_{Vdd} is that it takes a longer time to change V_{Vdd} levels than with smaller values. Typically, higher values of pseudo-resistance determine V_{Vdd} after about 4 time constants of sleep time. Considering these observations we choose R_{sp} as the pseudo-resistance at $V_{Vdd} = r_1$ for R_s.

F. Accuracy of the Model

(i) Heuristic approximation for R_s can impact V_{sleep}, a parameter which wakeup time and wakeup energy depend on. Hence sensitivity factors are derived to evaluate the impact of variations in V_{sleep} on T_{wu} and E_{wu}. Let S_{wt} and S_{we} denote sensitivities of wakeup time and wakeup energy to V_{sleep} respectively. By definition, $S_{wt} = \frac{\partial T_{wu}}{\partial V_{sleep}}$ and $S_{we} = \frac{\partial E_{wu}}{\partial V_{sleep}}$. From (13) and (15), the expressions for sensitivity factors are derived as,

$$S_{wt} = \frac{-R_{wu}C_L}{r_1 - V_{sleep}} \tag{23}$$

$$S_{we} = \frac{V_{dd}(V_{dd} - V_{sleep})C_L}{r_1 - V_{sleep}} \tag{24}$$

The bounds on variation of T_{wu} and E_{wu} with variation of V_{sleep} are thus obtained from

$$(\Delta T_{wu})_{max} = |S_{wt}|(\Delta V_{sleep})_{max} \tag{25}$$

$$(\Delta E_{wu})_{max} = S_{we}(\Delta V_{sleep})_{max} \tag{26}$$

In the next section, these equations are applied in the context of our experiments to determine variations of wakeup time and energy *w.r.t* errors in estimation of V_{sleep}.

(ii) It should be noted that in the derivation of model in wakeup mode, pseudo-resistance R_s was not considered because the effective resistance that contributes to the time constant of rising V_{Vdd} is determined by R_{wu} as opposed to sleep mode where R_s as a function of V_{Vdd} determines the falling rate. For brevity, a detailed analysis is omitted in this paper.

V. EXPERIMENTAL RESULTS

To validate the model and approximations proposed above we compare its application to four ISCAS benchmark circuits [11] listed in Table II with simulations using Spectre circuit simulator of Cadence Virtuoso ICFB. These circuits represent a maximum variation of about 9× in gate complexity and 11.5× in equivalent circuit capacitance between each other. We report detailed results for c6288 and c432 and provide a summary of results for the four circuits in Table VI.

	c7552	c6288	c499	c432
No. of NAND Gate Equivalents	1563	1504	354	182
Circuit Capacitance	2.892pF	3.171pF	0.6012pF	0.2742pF
Cells used for Synthesis	2-input NAND, 2-input NOR 2-input AND, 2-input XOR, Inverter Half Adder, Full Adder			

Table II
FEATURES OF ISCAS BENCHMARK CIRCUITS

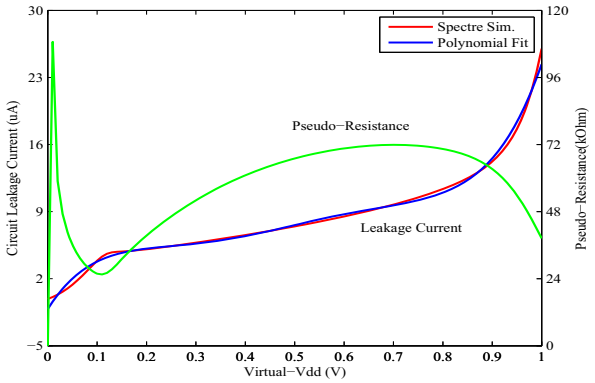

Figure 4. Variation of Circuit Leakage Current and Pseudo-Resistance with Virtual-V_{dd} in c6288

Each standard cell in Table II is characterized for leakage current for a supply voltage variation between 0 and 1V for all input patterns at an operating temperature of 100°C using Spectre. The standard cells are chosen from an industrial 65nm CMOS technology library. Each of these profiles are then fitted with polynomials using MATLAB. Hence, a leakage current profile is determined for the circuit by weighting the polynomials with number of occurrences in the gate netlist and adding them together to form I_{leak}. A leakage current profile for the circuit is shown in Fig. 4. From this curve, pseudo-resistance is determined at each point in the Virtual-V_{dd} segment. Fig. 4 shows such a variation for c6288.

For our simulations with Spectre, the supply voltage V_{dd} is set to 1.0V. The evolution of Virtual-V_{dd} during wakeup and sleep modes is shown in Fig. 5. In Table III, the maximum voltage levels attained by Virtual-V_{dd} with sleep transistors of different sizes for c6288 and c432 are given. Using the method described in section IV-A, they are determined to be within an error margin of 6mV (0.55%). Table IV shows results from Spectre simulations and application of (13) to determine wakeup time for different sleep transistor widths. It should be noted that the transistor widths considered are not designed to meet a particular peak current constraint [3] as we do not address the problem of logic clustering in this work. From Table IV we note that wakeup time has been determined within an error range of 17.6% for $W \leq 9.6\mu m$ in c6288. However, for $W > 9.6\mu m$ in c6288 and for the smaller circuit of c432, the relative errors are higher. We explain the observation as follows. In the first case the time constant $R_{lin}C_L$ is small due to small R_{lin} (Table I) whereas in the second case the time constants are small and comparable to the first case due to smaller load capacitance C_L (Table II). Evidently the rise time is lesser due to reduced time constants. At wakeup, due to presence of short circuit currents, the current through the sleep transistor varies. The effects of short circuit currents become more pronounced when the wakeup times are small, *i.e.,* when the time constants are small either due to large W (and hence smaller R_{lin}) or small C_L or both. The Virtual-V_{dd} voltage bounce observed in the evolution of V_{Vdd} with time in Fig. 5 is due this effect. In Table V wakeup energy computations with model in (15) are compared with Spectre simulations. A maximum error of 13.2% is observed across different transistor sizes and the two circuits. Table VI shows average errors in estimation of the three quantities across different transistor sizes for four circuits considered in this work.

W (μm)	r_1 (mV) Eq.(13)		Max. V_{Vdd} (mV) Spectre		Error (%)	
	c6288	c432	c6288	c432	c6288	c432
0.54	942.7	990.5	948.0	991.7	0.55	0.1
1.2	968.9	995.3	974.2	996.1	0.54	0.1
2.4	982.9	997.5	986.5	998.0	0.36	0.1
4.8	990.6	998.7	992.8	998.9	0.22	0.0
9.6	995.0	999.3	996.2	999.4	0.11	0.0
12	996.0	999.5	997.0	999.5	0.10	0.0

Table III
MAXIMUM VIRTUAL-V_{dd} AFTER WAKEUP

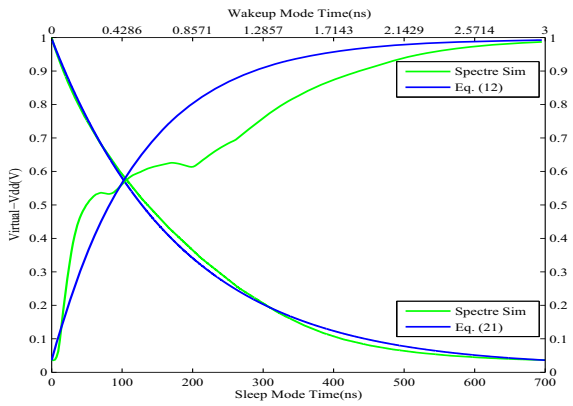

Figure 5. Virtual-V_{dd} in Wakeup and Sleep Modes (W=12μm) in c6288

In the sleep mode the maximum deviation of V_{Vdd} from Spectre simulations in c6288 and c432 has been 28.18mV and 56.67mV respectively. Both wakeup time and wakeup energy depend on V_{sleep} as shown in (13) and (15). From

W (μm)	T_{wu} (ns) Spectre		T_{wu} (ns) Eq. (13)		Error (%)	
	c6288	c432	c6288	c432	c6288	c432
0.54	46.8	3.95	46.89	4.06	0.2	2.8
1.2	22.3	1.95	22.14	1.92	0.7	1.5
2.4	12.1	0.984	11.26	1.246	6.9	26.6
4.8	6.58	0.648	5.867	0.516	10.8	20.4
9.6	3.68	0.444	3.033	0.272	17.6	38.7
12	3.09	0.395	2.439	0.220	21.1	44.4

Table IV
WAKEUP TIME COMPUTATIONS IN C6288 AND C432

W (μm)	E_{wu} (pJ) Spectre		E_{wu} (pJ) Eq. (15)		Error (%)	
	c6288	c432	c6288	c432	c6288	c432
0.54	3.871	0.259	3.84	0.284	0.8	9.8
1.2	3.721	0.258	3.541	0.281	4.8	8.6
2.4	3.607	0.261	3.376	0.280	6.4	7.2
4.8	3.598	0.266	3.277	0.280	8.9	5.2
9.6	3.669	0.273	3.228	0.283	12.0	3.6
12	3.705	0.275	3.217	0.285	13.2	3.6

Table V
WAKEUP ENERGY COMPUTATIONS IN C6288 AND C432

Circuit	Max. V_{Vdd} (%)	T_{wu} (%)	E_{wu} (%)
c7552	0.2	5.6	5.0
c6288	0.3	9.6	7.7
c499	0.05	21.3	14.9
c432	0.01	22.4	6.3

Table VI
AVERAGE ERRORS IN ESTIMATION OF MAXIMUM V_{Vdd}, WAKEUP TIME AND WAKEUP ENERGY IN ISCAS BENCHMARK CIRCUITS

(25) and (26), for an error in V_{sleep} of 100mV near $r_1 = 0.999V$ the change in T_{wu} is about $0.1R_{lin}C_L$ and the change in E_{wu} is $0.1C_L$. Therefore we infer that T_{wu} and E_{wu} are not significantly affected due to errors in estimation of V_{sleep}.

VI. CONCLUSION

In this paper, we have presented a model for Virtual-V_{dd} voltage from which wakeup time and wakeup energy of a power-gated logic cluster can be estimated. In active mode, steady state Virtual-V_{dd} can be used to determine leakage energy of the cluster. In sleep mode, the model can be used to estimate leakage energy savings in inactive states of the cluster due to power gating. In other words, key parameters used as optimization criteria for logic clustering have been captured in simple closed-form expressions.

Our simulations and application of the model to four ISCAS benchmark circuits with an industrial 65nm CMOS technology library show that on an average wakeup time and wakeup energy can be estimated within an error margin of 10% and 8% for larger logic blocks and within 22% and 15% error margins respectively for smaller logic clusters over $22\times$ variation in transistor sizes. The steady-state Virtual-V_{dd} is shown to be determined within 8mV (0.8%) of error. Coupled with sensitivity factors, error bounds can be determined for wakeup time to make design trade-offs for logic clustering. In future we propose to address wakeup time estimation errors at small time constants and use this model to determine energy savings in presence of wakeup overheads.

REFERENCES

[1] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, June 2003.

[2] M. Keating, D. Flynn, R. Aitken, A. Gibbons, and K. Shi, *Low Power Methodology Manual for System-on-Chip Design*. Springer, 2008, ch. Designing Power Gating.

[3] Y. Lee, D.-K. Jeong, and T. Kim, "Comprehensive Analysis and Control of Design Parameters for Power Gated Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, To appear.

[4] M.Anis, S.Areibi, and M.Elmasry, "Dynamic and Leakage Power Reduction in MTCMOS Circuits Using an Automated Gate Clustering Technique," in *Proceedings of the ACM/IEEE Design and Automation Conference*, New Orleans, June 2002, pp. 480–485.

[5] C. Long and L. He, "Distributed Sleep Transistor Network for Power Reduction," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 9, pp. 937–946, September 2004.

[6] A. Abdollahi, F. Fallah, and M. Pedram, "An Effective Power Mode Transition Technique in MTCMOS Circuits," in *Proceedings of the ACM/IEEE Design Automation Conference*, Anaheim, June 2005, pp. 27–32.

[7] Z. Hu, A. Buyuktosunoglu, V. Srinivasan, V. Zyuban, H. Jacobson, and P. Bose, "Microarchitectural Techniques for Power Gating of Execution Units," in *Proceedings of International Symposium on Low Power Electronics*, Newport Beach, USA, August 2004, pp. 32–37.

[8] S. Roy, N. Ranganathan, and S. Katkoori, "A Framework for Power-Gating Functional Units in Embedded Microprocessors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 11, pp. 1640–1649, November 2009.

[9] H. Singh, K. Agarwal, D. Sylvester, and K. J. Nowka, "Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 1215–1224, November 2007.

[10] H. Xu, R. Vemuri, and W.-B. Jone, "Dynamic Virtual Ground Voltage Estimation for Power Gating," in *Proceedings of the International Symposium on Low Power Electronics and Design*, Bangalore, August 2008, pp. 27–32.

[11] X. Lu, *Layout and Parasitic Information for ISCAS Circuits*. [Online]. Available: http://dropzone.tamu.edu/~xiang/iscas.html