Low Complexity On-Chip Distributed DC-DC Converter for Low Power WSN nodes

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***Abstract*—Supply voltage scaling has become an important low power technique to reduce the power consumption of sub-nanometer technologies. Instead of supplying same magnitude of V_{dd} for the whole chip, multi-V_{dd} and Dynamic Voltage Scaling (DVS) have been advocated for the enhanced power efficiency at the cost of added complexity. In this paper, we present a low area, low power on-chip DC-DC converter suitable for low power Wireless Sensor Network (WSN) nodes. This converter offers the flexibility to perform micro-level DVS for various blocks of the system. Peak efficiency of 90% has been achieved and the proposed DC-DC converter takes utmost delay of 30μs to switch between the different output voltages.**

I. Introduction

As the low power techniques are getting more sophisticated and refined in the recent years, the challenges in handling the power supply for low power systems has been constantly increasing [1]. Moreover these techniques are strongly motivated with the increasing interest of battery-powered devices like wireless sensor network nodes [2]. In the low power, battery-powered systems, the energy availability is limited and it has to be efficiently used to keep them functional for long time period. Lots of low power techniques have been addressed in the past to efficiently use the available power by reducing dynamic and leakage power components of the system. In sub-nanometer technologies, the percentage of the leakage power in the total power consumption is substantial [3] and techniques like power-gating are employed to reduce the leakage power [4].

Regarding dynamic power consumption, as the supply voltage is quadratically related to dynamic power, multi-V_{dd} and Dynamic Voltage Scaling (DVS) techniques are both used to scale the operating voltage to the possible minimum limit, which results in drastic dynamic power reduction. In multi-V_{dd}, various blocks of the system are supplied with different voltages with respect to their critical path timing, while DVS allows to tune the supply voltage during run time in order to meet the required performance and energy constraints of the running application.

DC-DC converters are used in DVS technique to convert the supply voltage from one level to another level. In general, DVS systems are equipped with off-chip voltage converters, because of the complexity in fabricating large inductors and capacitors inside the chip [5]. On the other hand, on-chip voltage converters are less complex and smaller in comparison with off-chip voltage converters. Though on-chip voltage converters are less complex, they are limited to low power applications due to limited output current driving capability. The distributed power delivery network as shown in Fig. 1, gives the advantage of applying DVS at the micro level for better power management [6], [7]. Also, voltage drop in the power network can be reduced by distributed power network due to the reduced load and localized power distribution [6].

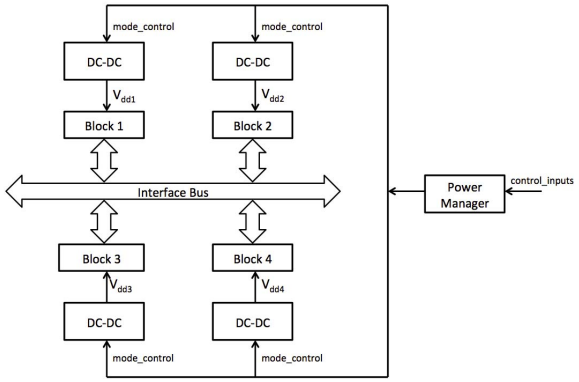

Fig. 1. General architecture of micro-level DVS in low power systems with on-chip DC-DC converters.

In this paper, we propose a low complexity, low power DC-DC converter suitable for low power systems like wireless sensor network (WSN) nodes. The paper is organized as follows. Section II presents related works and the proposed low complexity DC-DC architecture is described in Section III. Experimental results are given in Section IV, and finally Section V gives some conclusions and perspectives.

II. Related works

A. DC-DC converter

Previous works have studied and implemented on-chip switched capacitor DC-DC [6], differential amplifier based DC-DC [5], and fine grain DC-DC [7]. The switched capacitor network proposed in [6] consists of switches and capacitors to provide output voltage. In general, a switched capacitor DC-DC converter works in two phases, 1. Charging (ϕ1) and 2. Discharging (ϕ2). As shown in the Fig. 2 capacitors C_1 and C_2 are connected in series during the charging phase ϕ1, so that both the capacitors will be charged to half of the supply voltage. During ϕ2, the load is connected to the capacitors C_1 and C_2 which are connected in parallel. As the current

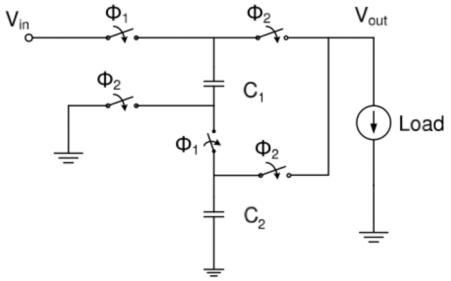

Fig. 2. Switched-capacitor based DC-DC converter [6].

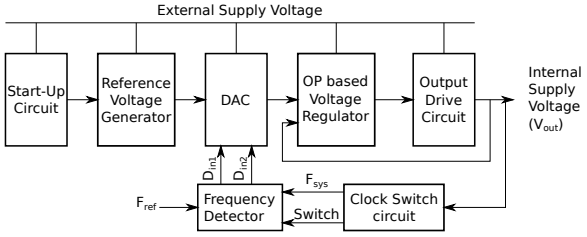

Fig. 3. Differential amplifier based DC-DC converter [5].

starts flowing, the capacitor will slowly loose its voltage and needs to be reconfigured in a regular time interval. With this method, more such switched capacitor circuits are required to produce different supply voltages for each of the blocks of the system. Also two-phase clock signals are required to charge and discharge the capacitor in a regular time interval. When such on-chip DC-DC converter scheme has to be employed for micro-level DVS in a system, the complexity of the system increases linearly with the number of required voltages. Also this DC-DC converter is not suitable when the area and complexity are one of the prime constraints.

In the differential amplifier based DC-DC proposed in [5], the reference voltage is varied using a DAC and a frequency detector is used to monitor the system clock to adjust the supply voltage as shown in Fig. 3. This method requires, DAC, frequency detector, clock switch, resulting in complex design and consumes more power. This kind of DC-DC converter is not suitable for battery powered applications, like WSN nodes.

In the fine grain DC-DC converter proposed in [7], the band gap circuit provides the reference voltage for all the DC-DC converters as shown in Fig. 4. Each DC-DC converter consists of a divider circuit, a source follower, a corrector, a sigma delta modulator, and a power stage circuit. The LC filter is constructed using discrete devices, a capacitor and an inductor. Sigma-delta modulator determines the switching frequency and the duty cycle based on the output current load. Again, this kind of DC-DC converter is more area consuming and not suitable for low power applications like WSN nodes.

In this work, we are proposing an on-chip DC-DC converter suitable for micro-level DVS in low power applications, which is simple in terms of design complexity with more or less same peak efficiency as in [5]-[7].

III. Proposed method

In this paper, we are proposing a DC-DC converter based on resistor voltage divider and multiplexer. In this method, we

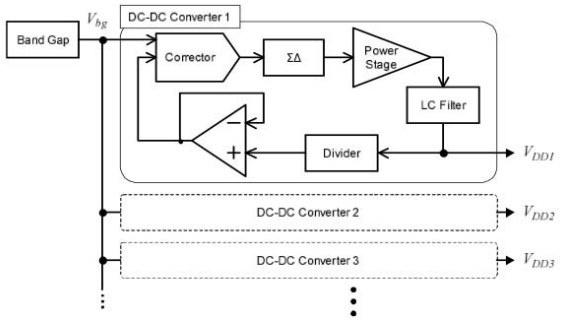

Fig. 4. Fine grain DC-DC converter for IP level DVS [7].

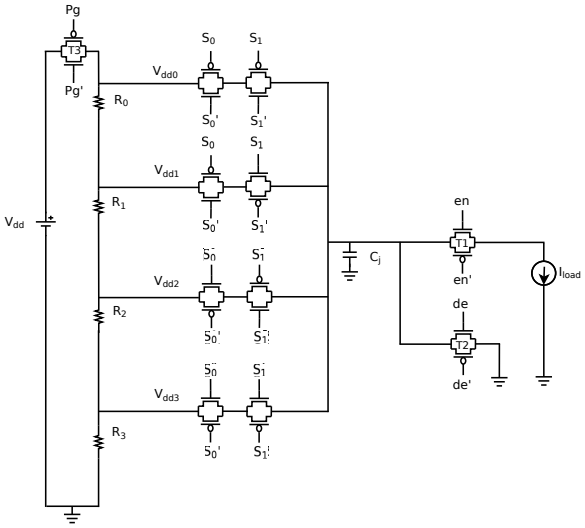

Fig. 5. Proposed low complexity on-chip DC-DC converter for low power applications.

are using the resistor voltage divider to produce the reference voltage for DVS technique. The output reference voltage produced from the resistor voltage divider is a fraction of the maximum supply voltage of the circuit. In the design shown in Fig. 5, all the resistors R_i are assumed to be of same resistance value; such that the supply voltage is divided into i equal parts irrespective of the value of the resistance. Capacitor C_j is used to store the voltage tapped from the resistor voltage divider. This is on-chip capacitor with higher Q factor and energy density. In order to charge quickly and also to increase the output current capability, the value of the resistors R_i has to be chosen small. Also the value of the capacitor has to be large enough to provide enough charge for the desired output current. The proposed DC-DC converter is focused for low power designs like WSN nodes, which are low current consuming loads in the order of few hundred nA to tens of μA.

In this circuit, I_{load} is the current sink, which depicts the load connected to the voltage regulator. I_{load} gives the maximum current driving capability of the voltage regulator. Control signals S_k are used to select the desired supply voltage level for the particular block of the system. Out of $2^k + 1$ possible power modes, two power modes are reserved for fully functional and power shut-off mode. When all 0's is

applied to the mode select lines (S_k), the fully-functional mode is activated with maximum supply voltage provided to the corresponding block of the system. Similarly minimum voltage mode can be activated by all 1's. Opening the switch $T3$ that disconnects the supply from the corresponding block of the circuit, can activate power shut-off mode. When the block is awaken, it will continue to work in the last selected power mode, unless the power mode is changed. Remaining $2^k + 1 - 2$ combinations of mode selection can be used to achieve various other power modes like sleep, memory-read, etc. Control signals are generated by a power manager block situated local to each block or global to the entire design, based on the granularity.

Based on the number of power modes n, an $n : 1$ multiplexer is constructed using transmission gates (TG). TG based multiplexer has the capability to faithfully pass the input voltage level to the output node, whereas multiplexers constructed using logic gates will pull up or down the output voltage. A transmission gate switch $T1$ as shown in the Fig. 5 isolates the multiplexer network and the load network. Initially, the load is disconnected from the DC-DC converter by opening the switch $T1$. This allows the capacitor C_j to get charged to the chosen supply voltage based on the mode selector S_k. The enable signal en is asserted after $5RC$ time (time required to fully charge the capacitor C_j) to bridge the load network with the DC-DC converter. The all 1's path of the multiplexer needs more time to charge the capacitor due to increased resistance, which determines the time for asserting enable signal en. When the supply voltage of a particular block needs to be changed, switch $T1$ is closed to safely disconnect the load from the DC-DC converter. Then the switch $T2$ is closed for a short time interval to discharge the capacitor C_j to the minimum supply voltage. Mode selector switches S_k are set in the right combination to charge the capacitor C_j to the chosen supply voltage. In this method, resistors in series with capacitor C_j will limit the input current until the capacitors are charged. The transmission gates in series with load network protects the load from inrush current and gives soft start-up.

Capacitor C_j in the circuit acts like a decoupling capacitor, which maintains the output voltage at a constant level for the varying output current. If the voltage from resistor voltage divider reduces due to increased current consumed by the load, the capacitor provides the energy to maintain the output voltage level. Also, if there is a sudden spike in the resistor output, the capacitor will be filtering the spikes by absorbing excess energy. Transistors in the transmission gate have to be sized properly to have low series ON resistance, so that it will not limit the output current. In this method, the time required to switch among various power modes is very minimal.

IV. Experiments and results

The proposed DC-DC converter has been tested using 28nm FDSOI technology. The input supply voltage of the resistive voltage divider is connected to clean and stable 1V voltage source. In this experiment, the peak current drawn by the load connected to DC-DC converter is 1μA. Therefore, the size of resistors R_i and capacitor C_j are chosen as 1KΩ and 1nF respectively to support peak output current of 1μA. In order to handle more load current, the values of the resistors and the capacitor have to be chosen carefully. The proposed DC-DC converter can deliver maximum output load current of 31μA, which means this converter can power around 7000 NAND gates at 20% switching activity. The maximum output current capability by the DC-DC converter is estimated based on the load-regulation test explained later in this section. In order to estimate the figure of merits of the proposed DC-DC converter, some pre-layout Spice simulations are carried out in Cadence Virtuoso environment using Spectre simulator under various PVT corners. The proposed DC-DC converter is used to supply some of the load like 4-tap FIR basic filter, 32-bit multiplier, chain of 100 inverters etc. In these simulations, long activity window (in the order of milli seconds) is used to determine the stability of the proposed DC-DC converter in different power modes for different loads.

Fig. 6 shows the waveform of output voltage from DC-DC converter which powers chain of 100 inverters. From the figure it is clearly evident, that the DC-DC converter is able to produce stable output voltage with the maximum voltage ripple of 10mV. Initially, the minimum voltage mode is set and selecting different power modes has gradually increased the output supply voltage. There are some strong voltage drops visible in between two different power modes, because the load is isolated from the DC-DC converter while changing the power mode. The maximum time required to change from one voltage to another is 30μs, which is considered to be a very tiny time interval for systems like wireless sensor network nodes.

Efficiency is one of the figure of merits used to characterize a DC-DC converter, and it is defined as the ratio of output power to input power [8]. In this proposed method, the DC-DC converter behaves more or less like a linear voltage regulator. Since the output current is drawn from the input supply voltage through resistors, the magnitude of the input current is same as that of the output current. Therefore the efficiency of this DC-DC is the ratio between output and input voltage. When the difference between input and output voltages is small, maximum efficiency of 90% can be achieved. The peak efficiency achieved by the proposed method is more or less equivalent to the peak efficiency of 91.88% and 95.38% as proposed in [7], [6] respectively, but with a low complexity and area. Table I, shows the complexity comparsion in terms of number of basic components required to construct a DC-DC converter which can provide 4 different output voltages. The comparison has been done only between the proposed DC-DC converter and the switched capacitor based converter proposed in [6], as the other two converters proposed in [5], [7] are deemed to be complex based on their architecture shown in the Figs. 3 and 4 respectively. The resistors in the proposed methods are realized using transistors and the approximate area consumed by 26 transistors is approximately 1.85μm^2 in 28nm FDSOI technology. Power consumption of the proposed DC-DC converter is mainly due to the loss in the resistors, for the maximum output current of 31μA, the maximum power consumption is 5.7μW.

TABLE I. Complexity comparison of DC-DC converters which can provide 4 different voltages

DC-DC Converter	No. of transistors	No. of capacitors
Proposed DC-DC	26	1
DC-DC proposed in [6]	52	10

Load regulation is another figure of merit, which charac-

TABLE II. DC-DC CONVERTER COMPARISON IN THE CONTEXT OF LOW POWER WSN NODES.

DC-DC Methods	Technology	Complexity	Flexibility	Peak Efficiency	Max. Voltage ripple	Max. Output Current
Proposed DC-DC	28nm FDSOI	Low	High	90%	10mV	31μA
Switched capacitor DC-DC[6]	32nm CMOS	Medium	Low	95.3%	17mV	-
On-chip DC-DC [5]	130nm CMOS	High	Medium	-	5mV	100mA
On-chip DC-DC [7]	65nm CMOS	High	Medium	91.88%	10mV	100mA

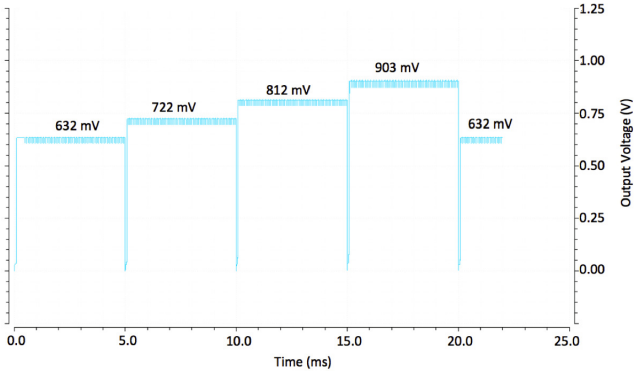

Fig. 6. Output voltage from DC-DC converter which powers the chain of 100 inverters

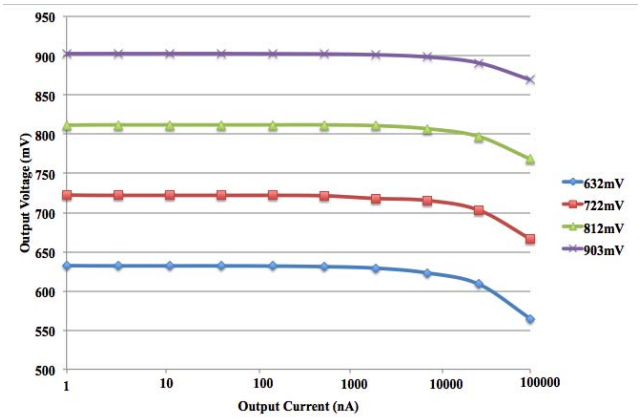

Fig. 7. Plot of output voltage vs. output current for various output voltage values shown in the legends

terizes a DC-DC converter's ability to maintain the specified output voltage as the output current I_{load} varies [8]. Fig. 7 shows the graph of load regulation test performed over the range of load currents for different output voltages. From Fig. 7 it is evident that the proposed DC-DC is able to maintain stable output voltage over the range of output current loads. Based on the tolerable voltage drop of 10mV, the maximum output current capability of the DC-DC converter is determined from the graph. Table II, shows the overall comparison of the proposed DC-DC converter with the other DC-DC converters proposed in [5]-[7]. From Table II, it is evident that the proposed DC-DC method is less complex and offers more flexibility for low current WSN node applications with the efficiency closer to the methods proposed in [5]-[7]. The maximum output current capability of DC-DC converters proposed in [5], [7] are 100mA, whereas the proposed DC-DC converter can only provide maximum output current of 31μA, which is sufficient to handle the smaller blocks in the low power applications.

V. CONCLUSION

In this paper, we have proposed and experimented an on-chip DC-DC converter for low power applications like WSN nodes. The proposed circuit consumes less area and can be easily fabricated on-chip for distributed power delivery network. Maximum efficiency of 90% can be achieved with the maximum latency of 30μs to change the output from the minimum voltage to maximum voltage in the proposed method. This design offers stable output voltage for a range of output currents from 1nA to 31μA as required for low power applications like wireless sensor network nodes. Micro-level Dynamic Voltage Scaling and Power Gating can therefore be easily implemented with using this converter in low power applications like sensor network nodes.

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