Design and Implementation of WCDMA Platforms : Challenges and Trade-offs*

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ABSTRACT

The purpose of this paper is to present the results and the analysis of the implementation of WCDMA applications into programmable and reconfigurable platforms. WCDMA is integrated in the third-generation radio communication systems and represents one of the more complex part in term of computation needs. We consider in this paper the implementation of transmitter and receiver algorithms. The structure of the WCDMA receiver is mainly based on a FIR reception filter, and a rake receiver with synchronization mechanisms. The complexity of the different algorithms of WCDMA are detailed to show the hard real-time constraints implied by this application.

We show the implementation results of the WCDMA transmitter and receiver on three different platforms: a high-performance VLIW DSP, a reconfigurable FPGA device (Xilinx Virtex E) and a functional-level reconfigurable architecture (DART). We propose a new methodology that allows to transform the floating-point description of the different processing algorithms into a fixed-point implementation under a strict control of the performances. Finally, the results of these different implementations are discussed in term of energy efficiency, performances and cost.

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1. INTRODUCTION

The third generation of wireless communication device is an important challenge for the next two or three years because the technology of this new generation is far more complex than the second generation. The WCDMA standard [8], approved by the European Telecommunications Standards Institute (ETSI) seems to be a good candidate for the future Universal Mobile Telecommunications System (UMTS). WCDMA uses a wide frequency band of 5 MHz at 2 GHz. The multiplication of the original signal by a pseudo random sequence at a higher rate called the Chip Rate in the digital modulator stage leads to the spreading of the spectrum and enables the sharing of the same frequency band by many users. In the receiver the despreading allows the recovering of the original signal. The transmitted signal is similar to random noise and is difficult to demodulate. The receiver is of a higher complexity than the transmitter because of interfering signals due to environmental effects: attenuation, fading, doppler and multipath due to reflections. A solution to improve the reception is the rake receiver method which consists in a computation of the different delayed copies of the received signal and the combination of the different results. Price and low power are among the most important criteria for the market of portable products, these constraints lead to utilize fixed-point architecture rather than floating-point architectures.

For the different platforms we compare and discuss the results of the implementation of various algorithms from the WCDMA application. In the section 2, the structure of the WCDMA receiver is detailed. The process followed for the obtention of the receiver fixed-point specification is summarized in the section 3. After the presentation of the available processing alternatives, the results obtained for the different implementations are presented in the section 4. We show the implementation results of the WCDMA transmitter and receiver (rake receiver, receiver filter, ...) on three different platforms. One of them comes from the programmable domain, by the use of a high-performance DSP (TMS320C64x) based on a VLIW structure. The other two come from the reconfigurable domain at different level of granularity. We consider results on reconfigurable platforms including

a fine-grained reconfigurable device (Xilinx Virtex 2000-E) and a coarse grain reconfigurable architecture (DART [3, 4]) which is designed for low-power computing. Finally, we focus on the implementation trade-offs between the different platforms in terms of energy efficiency, performances and cost.

2. WCDMA REQUIREMENTS

The European UMTS is based on the Wide band Code Division Multiple Access (WCDMA) technique. The bandwidth of the transmitted signal is equal to 5MHz. The frequency of the code corresponding to the chip rate (F_{chip}) is fixed to 3.840 MHz. A QPSK modulation associated with a root raised impulse shaping filter with a roll-off factor of 0.22 is used. The transmitter interfaces for up and downlink are slightly different. A physical channel is defined by a spreading code. The spreading factor can take a set of values $N_s = 2^k$ with $k \in \{2, 3.., 9\}$, leading to different data rates for spreading factors from 4 to 512. Each physical channel associates information data (DPDCH) and control data (DPCCH). The channel bits are split to the *In-phase* and the *In-quadrature* branches, then spread with an orthogonal variable spreading factor code (OVSF), and then scrambled by a specific spreading sequence (Kasami codes). On the downlink, all users share the same scrambling sequence so the OVSF codes are used to separate the different channels because the orthogonality properties lead to a null intercorrelation when the codes are synchronized.

The reception filter and rake receiver are the most critical element in the implementation of the receiver. The reception filter is made up of two real FIR filters processing the in-phase and in-quadrature input over-sampled signals. The complexity of this reception filter is equal to

$$\mathcal{C}_{FIR} = 2.N_{FIR}.N_{os}.F_{chip}\ (MAC/s) \tag{1}$$

N_{FIR} corresponds to the number of taps and N_{os} represents the over-sampling factor. For our implementation, the FIR filter is made up of 64 taps. Thus the complexity of the reception filter is closed to 2 $GMAC/s$, for an over-sampling factor N_{os} equal to 4.

The complex received signal s_e is made up of different delayed copies of the transmitted signal s_m and of an additive noise $w(n)$. If L' delayed replicas of the received signal for a number M of users are considered, the value of the signal $s(n)$ at the output of the reception filter is

$$s_e(n) = \sum_{m=1}^{M} \sum_{l=1}^{L'} s_m(n - \tau_l) + w(n) \tag{2}$$

The concept of the rake receiver is based on the combination of the different multipath components in order to improve the quality of the decision on the symbol. Each multipath

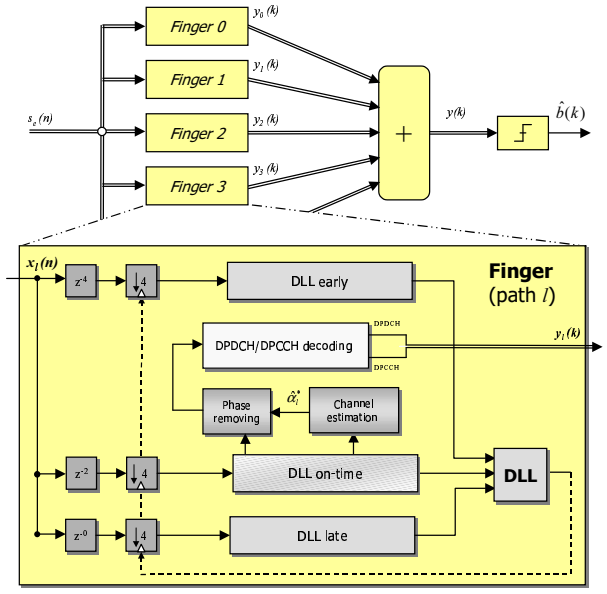

Figure 1: Principle of the rake receiver

signal is processed by a finger which correlates the received signal by a spreading code aligned with the delay τ_l of the multipath signal. The multipath components can be considered as uncorrelated when the delay exceeds a chip period. Demodulation results of a weighted decision at the outputs of the correlators. Using the maximum likelihood criteria the symbol is estimated from the $y(k)$ signal

$$y(k) = \sum_{l=1}^{L} y_l(k) = \sum_{l=1}^{L} \alpha_l^*(k) r_l(k) \tag{3}$$

The structure of the rake receiver and the different fingers is detailed in the figure 1. The signal $y(k)$ corresponds to the combination of the different finger outputs $y_l(k)$. In order to combine the results of the different fingers, the complex amplitude α_l of the l^{th} path must be estimated and removed. The symbols are decoded by multiplying the received signal with a synchronized version of the code generated in the receiver. The synchronization of the code and the received signal is made with a Delay-Locked Loop (DLL). The rake fingers must be reallocated when delays change of more than a chip delay but small changes are processed by this code tracking loop.

For each finger, the symbols (DPDCH/DPCCH) are estimated with the structure presented at the figure 2. Thanks to the complex multiplication of the received signal by the conjugate of the Kasami code the unscrambling operation is performed. Then the phase distortion resulting of the transmission channel needs to be removed. At last the despreading operation from OVSF code transforms the wide band received signal into a narrow band signal.

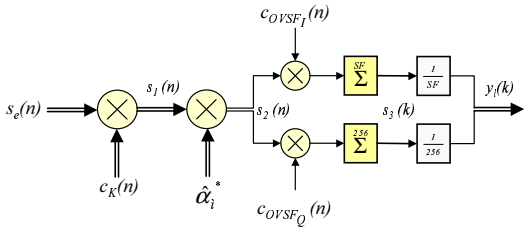

Figure 2: DPDCH/DPCCH decoding

System simulations under Matlab have been done and a mixed C-SystemC model has been developed to validate the full uplink and downlink simulations in floating and fixed-point formats. For our experiments, we choose the different parameters previously described (64-tap filters, 3.84 MHz chip frequency, over-sampling factor of 4) and a number of $L = 6$ fingers for the rake receiver.

3. FIXED-POINT SPECIFICATION DETERMINATION

Most digital signal processing algorithms are specified with floating-point data types but they are finally implemented in fixed-point architectures in order to satisfy the cost and power consumption constraints of embedded systems. For determining automatically the fixed-point specification of the WCDMA receiver, the methodology presented in [6] has been used. This new methodology allows to implement a floating-point algorithm into a fixed-point architecture under accuracy constraint. This accuracy constraint is evaluated with a single metric which is the Signal to Quantization Noise Ratio (SQNR). A technique for determining automatically the analytical expression of the SQNR has been proposed [7]. This analytical approach allows to reduce dramatically the execution time of the fixed-point format optimisation process compare to a fixed-point simulation based approach. Indeed, in this case, a new simulation is required when a fixed-point data format is modified.

The accuracy constraint corresponding to the minimal value of the SQNR ($SQNR_{min}$) is defined according to the performance constraints of the system. In the case of the WCDMA receiver, the performances are specified through the maximal value of the bit error rate (BER). The accuracy constraint has been defined such as the system output BER is not modified after the fixed-point conversion process. The minimal value of the SQNR is obtained with a floating-point simulation as shown in figure 3. The error due to the fixed-point conversion is modelized by a noise source b_y located at the output of the system. The power of this noise source is increased as long as the BER is not modified. The minimal value of the SQNR is obtained from the maximal value of the noise power which allows to fulfill the BER constraint. Then, the fixed-point specification is determined in order to optimize the implementation and to fulfill the accuracy constraint. This optimized fixed-point specification is simulated in order to verify if the maximal BER constraint is still fulfilled. In the opposite case, the minimal value of the SQNR is adjusted and the floating-point to fixed-point process is repeated. With this approach, only few fixed-point simulations are required. For the WCDMA receiver, this accuracy constraint determination process leads to a minimal value of the SQNR equal to 12.5 dB.

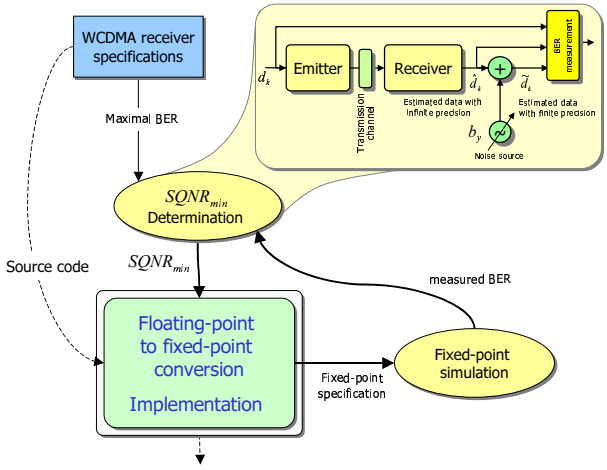

Figure 3: Global approach for the accuracy constraint determination and floating-point to fixed-point conversion

The high-frequency signal coming from the antenna is converted into a baseband one and then digitalized with an Analog-Digital Converter (ADC). An automatic gain control system is used in order to maintain the power of the ADC input signal and to exploit all the dynamic range offered by the ADC. The influence of the ADC word-length on the receiver performance has been studied in [8]. The results show that the degradation due to the ADC word-length can be neglected when this word-length is greater than 6 bits. Thus, the word-length of the WCDMA receiver is fixed to 8 bits and the fixed-point specification is determined with the SQNR constraint. For the FIR filter, the word-length of the input and output are equal to 8 bits and the computation are achieved in double precision. In this case, the word-length of the addition and the multiplication output is equal to the double of the word-length of the multiplication input. Thus, no bit is eliminated during the multiply-accumulate operations. For the rake receiver, the word-length of the different data for the DPDCH/DPCCH decoding, presented in the figure 2, is given in table 1. Except for the first complex multiplication the other operations are achieved in single precision. In this case, the word-lengths of the multiplication output and input are equal. Thus, the least significant bits of the multiplication output are eliminated.

Data	s_e	s_1	s_2	s_3	y
Word-length (bits)	8	16	16	16	16

Table 1: Rake receiver data word-length

4. WCDMA IMPLEMENTATIONS

4.1 Processing Alternatives

Generally a new standard is proposed when it is possible to implement it in ASICs, later with improvements of technologies it becomes possible to implement it in DSPs, nevertheless flexibility and reusability are very important for an evolving new standard. The most flexible platforms are the software programmable components like microprocessors and DSPs. The complexity of wireless systems is growing quicker than the capabilities of silicon predicted by Moore's law, fortunately most of these algorithms can efficiently be parallelized [10]. The key issue in the design of third generation radio communication systems is to find a good balance between flexibility and high-processing power on one side, and area and energy-efficiency of the implementation on the other side [10]. The purpose is to implement an efficient WCDMA system using programmable and reconfigurable logic like FPGAs, DSPs and ASICs, and to compare the performances. We show the implementation results of the WCDMA transmitter and receiver (rake receiver, transmitter and receiver filters, ...) on three different platforms. The rake receiver correlates the received data with the spreading code. For a number K of fingers when the receiver operates at the chip frequency set by the spreading code it must process K times the chip frequency.

The power savings resulting from ASIC implementations have a significant advantage over DSPs but there is an important drawback when the product life cycle is short because of the long design time cycle for ASIC. However, the enhancement of DSP in terms of power consumption, reduction of code size, specialized instructions for wireless technology reduces differences between DSP and ASIC solutions [4]. Other improvements for DSP are VLIW (Very Long Instruction Words) processors exploiting Instruction Level Parallelism and leading to a more efficient compilation of high level code (TMS320C6x) or Static Superscalar Architectures which do not require sophisticated timing prediction (TigerSHARC). The more efficient approach seems to be reconfigurable architectures. Many projects are based on the use of FPGA, sometimes associated with a programmable processor. Some of these architectures are low-power, other very flexible or powerful, but none of them associates all requirements needed by 3G communications terminals.

Different approaches have been published. A.M. Shankiti and M. Leeser [11] investigate mapping a rake receiver to Xilinx XCV50 Virtex chip. Their choice of FPGA is supported by a literature review. When comparing the performances of algorithms implementations for FPGA and DSP, flexibility, good communications, the ability to match the implementation to the algorithm, concurrent processing capabilities, the result is that FPGA implementations usually outperform DSP implementations. As an example they propose the American IS95 protocol for CDMA communications (frequency 1900MHz, bandwidth 1.25 MHz) which needs for demodulating and despreading the signal the processing of 1.25 million samples each second. For a FPGA running at 10 MHz each sample requires 2 multiplications (phase and quadrature), with 2 multipliers, 8 cycles are available for each multiplication. They conclude that this design can be easily implementable while fitting several fingers per chip. We propose the implementation of the transmitter and receiver filters and of the rake receiver mapped to a Xilinx Virtex 2000-E.

The Berkeley Pleiade model [12, 10] combines core processors, DSP, programmable logic, embedded memory connected by a reconfigurable communication network. This results in a SOC (System On a Chip) composed of different interconnected embedded processors each of these is optimized for particular models of computation. Their approach combines high-performance, energy efficiency and flexibility and deals with multiple programmability levels. The efficiency of reconfigurable devices is highly dependant of the methodology and of the tools provided to support their architectures.

We proposed the DART architecture [3, 4] designed in collaboration with the University of Brest and STMicroelectronics to get the programming model as simple as possible. The development tool stems from a retargetable compiler (CALIFE [1]) developed at IRISA in the R2D2 project and from our behavioral synthesis framework BSS [5]. Measuring performances of these various implementations can be standardized using the million-multiply-accumulates-per-second (MMACS).

4.2 FPGA Architecture

A FPGA device is made of an array of highly configurable resources. Fine-grained and coarse-grained configurable logic blocks (CLBs) can be defined to directly implement in hardware a digital processing algorithm. Another alternative consists in including DSP cores as an IP in an FPGA, leading to efficient system-on-chip solutions. A lot of works has started demonstrating the advantages of using FPGAs in signal processing systems. For example in [9, 2], authors demonstrate on relatively old technology that FPGAs provide advantages in flexibility and performance comparing to DSP and ASIC solutions. New generations of reconfigurable circuits improve these benefits. For example, Virtex architecture includes an array of CLBs (implementing up to 2 million equivalent gates), embedded blocks of ram (BRAMs), and configurable I/O blocks (IOBs). The Virtex II family provides very useful enhancements for software radio implementations like higher density and dedicated 18-bit×18-bit multipliers.

The implementation of the 64-tap receiver filter, for a signal processed at the chip frequency (rate) 3.84 MHz (260 ns) and an over-sampling of 4, leads to a solution running at 25 MHZ and using 5% of the resources (1094 slices including 512 flip-flops) on a Virtex-2000E. This solution has been obtained with Synplify Pro synthesis tools from Synplicity and Place and Route from Xilinx. The high sampling frequency of the filter could be achieved by the use of an extensive specialization of the operators and a strong parallelization

of the algorithm. The execution time of the filter is 38.6 ns and consumes a power of 919 mW.

In the worst case of a spreading factor equal to $SF = 256$, a symbol must be decoded with the rake receiver in less than 66.6 μs. To achieve this constraint, we have synthesized a C specification of the application using the high-level synthesis framework (BSS) developed in our project. Then, FPGA synthesis has been performed to obtain the following results. The implementation of a rake receiver with 6 fingers leads to a total of 300 slices (50 slices per finger). The receiver also uses 20 Kbit of embedded SRAM memory.

4.3 The DART Architecture

The DART architecture paradigm is a functional level reconfigurable architecture. Two kinds of operators are integrated in this architecture for computations at different levels of granularity. Bit level operations use a FPGA core while arithmetic processing uses dynamically Reconfigurable DataPaths (DPR) in order to optimize the architecture according to the application. The arithmetic processing primitives are the DPRs, each comprises 4 units with its own address generation for a local memory (256×16 bits), 2 multipliers/adders (16×16 bits $\rightarrow$ 32 bits), 2 ALUs (32+40 $\rightarrow$ 40), and 2 registers all interconnected via a powerful communication network. These processing primitives are integrated within the clusters of DART. The cluster controller manages the configuration of 6 DPRs and an FPGA, while all DPRs share a common data memory via a memory controller.

Moreover, SWP (Sub Word Parallelism, also referred as SIMD) capabilities have been included in order to exploit the data level parallelism. An operator (multiplier, adder, shifter) of word-length N is split in order to execute k operations in parallel on sub-word of word-length N/k. Thus, this architecture can manipulate a wide diversity of data types (8, 16, 32, 40 bits).

At the system level DART architecture may encompass 4 clusters, an instruction memory, a data memory, a configuration memory, an I/O controller and a task controller. The FPGA core of each cluster is very effective for the generation of Gold or Kasami code in WCDMA processings. The cluster controller manages sequences configurations, it does not need to access to the memory at every cycle but only when a reconfiguration occurs, allowing significant energy savings. Some reconfigurations dealing with regular processing are realized for long periods of time, some others are not regular and implies different processing from a cycle to an other. The address generation units, in order to be efficient in a large variety of applications, support many addressing pattern like bit-reverse, modulo, pre/post increment. This unit enters a sleep mode when no address has to be generated in order to minimize energy consumption. The evaluation of the performance relies on Synopsys' `Design Compiler` tool for the VLSI synthesis and on a DART simulator developed in SystemC. The synthesis of the DPR estimates the operating frequency at 130 MHz on 0.18 μm CMOS technology. When handling 16-bit data, each DPR provides 260 MMACs leading to 1.56 GMACs for a cluster of 6 DPRs.

The implementation into one cluster of the reception filter based on two 64-tap FIR filter, leads to the use of this cluster 82% of the execution time. A rake receiver made up of 6 fingers, has been implemented into a cluster. For this algorithm, the cluster usage rate is equal to 8.9%. Several architectures can reach the same level of performance but DART is more efficient in terms of energy. The efficiency is obtain by a minimization of memory accesses and by a scaling of the voltage operating frequency of the clusters according to the complexity of the different tasks. The energy efficiency of the overall cluster is around 33 MOPS/mW for the reception filter and the rake receiver, leading to a total energy consumption of 76mW.

4.4 VLIW DSP Architecture

The C62x devices are VLIW 32-bit fixed-point processor clocked from 150 to 300 MHz, computing 8 instructions per cycle in 8 independent functional units (1200-2400 MIPS). The processor has 32 general-purpose registers of 32-bit word length. The eight functional units provide six arithmetic logic units (32/40 bits) for a high degree of parallelism and two 16-bit multipliers for a 32-bit result. It uses a load store architecture and provides internal program and data memory. It also uses a code compression system. The complete development tool is provided by TI. The C64x devices (300-600 MHz) are an enhanced version of the 62x devices, increasing processing performances (2400-4800 MIPS) and lowering energy consumption. Moreover, SIMD (i.e. SWP) capabilities have been included in order to exploit the data level parallelism. Thus, this processor can manipulate a wide diversity of data types (8, 16, 32, 40, 64 bits).

Given the complexity of the reception filter (2 $GMAC/s$), only hardware implementations lead to efficient solutions. Indeed, the FIR filter output sample must be computed in less than 65 ns. In the best case, with a 300 MHz C64x, the execution time of the reception filter is equal to 213 ns.

A rake receiver finger has been implemented into the C64x and C62x DSPs. For the C64x, the SIMD capabilities have been investigated in order to reduce the execution time by achieving several operations in parallel on the same operator. The C code describing the finger contains the synchronization of the code with the DLL, the estimation of the complex amplitude of the multipath and the decoding of the symbols. The results, presented in the table 2, give the number of cycles and the processing time at 300 MHz required for processing one chip in a finger, the processor usage rate for the rake receiver and the average number of instructions executed per cycle (IPC).

The C64x can execute up to 8 classical instructions per cycle. The use of the C64x SIMD capabilities allows to reduce the execution time of the code of a factor closed to 2.5. The real-time execution of a rake receiver made up of six fingers in the 300 MHz C64x uses the processor 39.3 % of the time

if SIMD capabilities are taken into account. Thus, in the case of a base station two users can be processed with one C64x DSP.

Processors	C64x		C62x
	no SIMD	*SIMD*	
Processing time of 1 chip for a finger (cycles)	**12.23**	**5.12**	**12.23**
Processing time of 1 chip for a finger (ns)	**40.7**	**17**	**40.7**
Instructions Per Cycle (IPC) for a finger	**5.3**	**5.8**	**5.3**
Processor usage rate for the rake receiver	**94%**	**39.3%**	**94%**

Table 2: Implementation results of the WCDMA rake receiver in VLIW DSP. The execution time are given for a processor clock of 300 MHz

5. CONCLUSION

For the design of 3G systems ASIC do not provide the necessary flexibility. High performance DSP based on VLIW structure offer the flexibility required by 3G systems and allow to implement a rake receiver. Nevertheless, the energy efficiency of this kind of DSP is too low for a mobile station. In the case of a base station the number of users proceeded per DSP is still too low for providing a viable solution in terms of cost.

The best approach seems to be reconfigurable architectures, FPGAs bring both flexibility and performances but are not power efficient and remain the most expensive solution. Custom Fit and reconfigurable processors associate low power, high performances, flexibility at a fair price. In this field, DART with the help of efficient methodologies and design tools allowing dynamic reconfiguration will meet the requirements for effective hardware platforms.

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